ST17H69

Bluetooth LE 5.2 +Zigbee 3.0 Multi-protocol System on 24bit ADC chip

Key Features

- ARM® Cortex™-M0 32-bit processor
- Memory
  - 128KB-8MB in-system flash memory
  - 64KB SRAM, all programmable retention in sleep mode
  - 4-way instruction cache with 8KB Cache RAM
  - 96KB ROM
  - 256bit efuse
- 49 general purpose I/O pins
  - GPIO status retention in off/sleep mode
  - Can be configurable as serial interface and programmable IO MUX function mapping
  - Can be configured for wake-up
  - Support triggering interrupt
  - 3 quadrature decoder(QDEC)
  - 6-channel PWM
  - 2-channel PDM/I2C/SPI/UART
  - 4-channel DMA
  - LCD driver supports 4COMx31SEG or 3COMx32SEG, 1/3 bias
- DMIC/AMIC with microphone bias
- 8-channel 12bit ADC with low noise voice PGA
- **24bit Σ-Δ ADC, maximum ENOB 22.6 bits**
- 6-channel 32bit timer, one watchdog timer
- Real timer counter (RTC)
- Power, clock, reset controller
- Flexible power management
  - Operating Voltage range 2.4V to 3.6V
  - Embedded buck DC-DC and LDOs
  - Battery monitor
- Power consumption
  - 0.3uA @ OFF Mode (IO wake up only)
  - 1uA @ Sleep Mode with 32KHz RTC
  - 13uA @ Sleep Mode with 32KHz RTC and all SRAM retention
  - Receive mode: 4mA @3.3V power supply
  - Transmit mode: 4.6mA (0dBm output power) @3.3V power supply
  - MCU: <60uA/MHz
- RC oscillator hardware calibrations
  - Internal High/Low frequency RC osc
  - 32KHz RC osc for RTC with +/-500ppm accuracy
  - 32MHz RC osc for HCLK with 3% accuracy
- High Speed Throughput
  - Support BLE 2Mbps Protocol
  - Support Data Length Extension
  - Throughput up to 1.6Mbps(DLE+2Mbps)
- Support SIG-Mesh Multi-Feature
  - Friend Node/Low Power Node/ Proxy Node/Relay Node
- 2.4 GHz transceiver
  - Compliant to Bluetooth 5.2
  - Sensitivity:
    -99dBm@BLE 1Mbps data rate
    -105dBm@BLE 125Kbps data rate
    -103dBm@Zigbee 3.0 250Kbps data rate
  - TX Power -20 to +10dBm in 3dB steps
  - Single-pin antenna: no RF matching or RX/TX switching required
  - RSSI (1dB resolution)
  - Antenna array and optional off-chip RF PA/LNA control interface
- AES-128 encryption hardware
- Link layer hardware
  - Automatic packet assembly
  - Automatic packet detection and validation
  - Auto Re-transmit
  - Auto ACK
  - Hardware Address Matching
  - Random number generator
- Operating temperature:
  - -40˚C ~+85 ˚C
- RoHS Package: QFN64(8mm x 8mm)
- Applications: wearables, beacons, home and building, health and medical, blood pressure meter, Infrared temperature measurement,Weight scale , High-precision measurement, data acquisition,industrial and manufacturing, data transmission, PC/mobile/TV peripherals, internet of things (IoT)

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Revision History

Date	Version	Description
2021.11	1.0	First Edition.
2021.12	1.1	24bit Σ-Δ ADC, maximum ENOB 22.6 bits

Table of Contents

1 Introduction

ST17H69 is a System on Chip (SoC) for Bluetooth LE 5.2 applications. It has ARM® Cortex™-M0 32-bit processer with 64K retention SRAM, 128KB-8MB flash, 96KB ROM, 256bit efuse, and an ultra-low power, high performance, multi-mode radio. Also, ST17H69 can support BLE with security, application and over-the-air download update. Serial peripheral IO and integrated application IP enables customer product to be built with minimum bill-of-material (BOM) cost.

2 Product Overview

2.1 Block Diagram

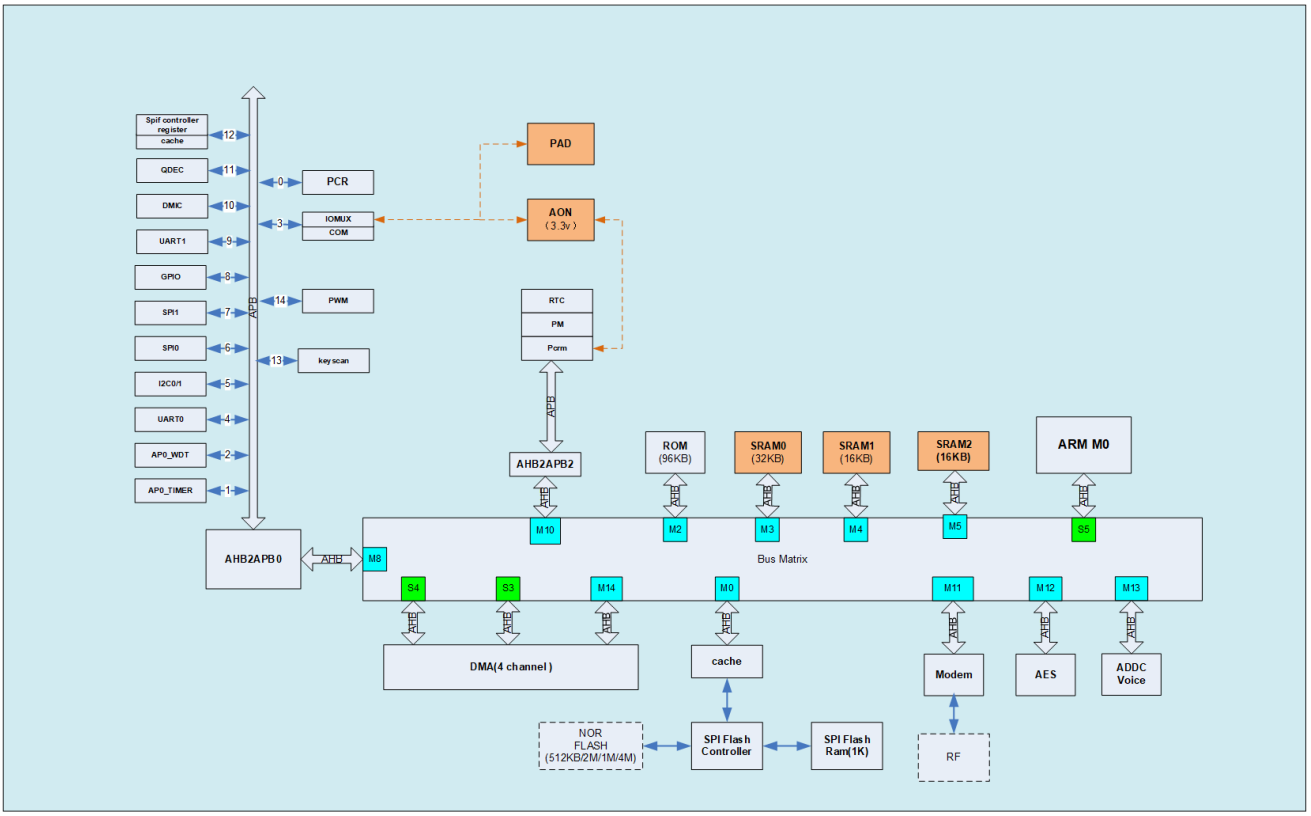

Figure 1: ST17H69 block diagram

2.2 Pin Assignments and Functions

This section describes the pin assignment and the pin functions for the package type of QFN64.

2.2.1 ST17H69 (QFN64)

2.2.1.1 Pin Assignment

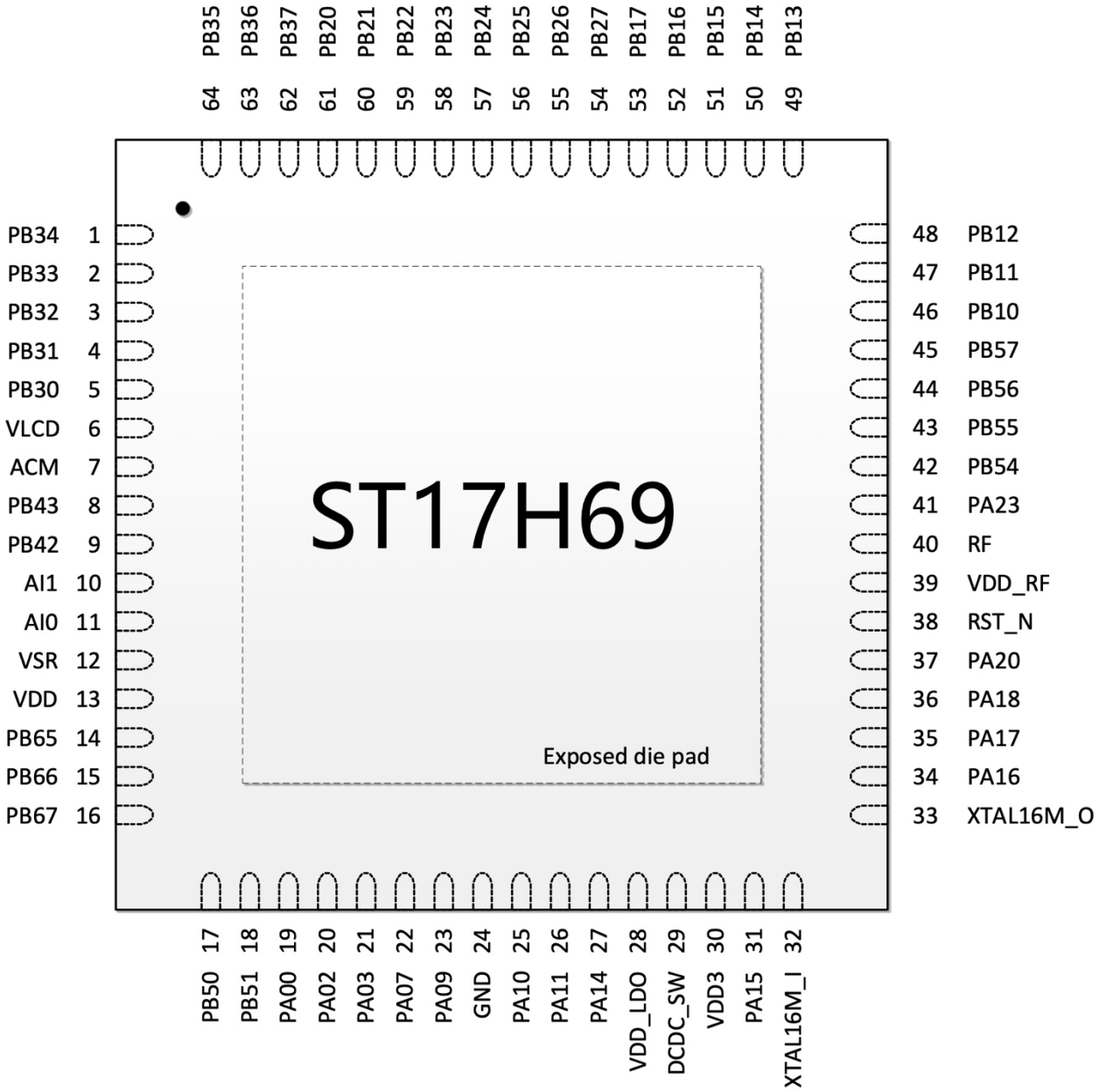

Figure 2: Pin assignment – ST17H69 QFN64 package

2.2.1.2 Pin Functions

Pin	Pin name	Description
1	PB34/SEG1	SEG1，数字 IO，复用 SEG1
2	PB33/COM3/SEG0/SCK*	数字 IO，复用 COM3（1/4DUTY）或 SEG0（1/3DUTY），复用 SPI 接口 SCK
3	PB32/COM2/SDI*	数字 IO，复用 COM2，复用 SPI 的 SDI
4	PB31/COM1/SDO*	数字 IO，复用 COM1，复用 SPI 的 SDO:
5	PB30/COM0*	数字 IO，复用 COM0
6	VLCD	LCD 的驱动电源，外接 1uF 电容到 VSS
7	ACM	内部基准或 VSR 的分压输出，可以作为模拟共模电压
8	PB43/AI3/Touch2/INT2/LVDIN2	数字 I/O，复用 ADC 输入 AI3，复用触摸按键 2，复用外部中断 2，复用外部电 压检测通道 2
9	PB42/AI2	数字 I/O，复用 ADC 输入 AI2
10	AI1	ADC 输入 AI1
11	AI0	ADC 输入 AI0
12	VSR	内部稳压源输出，用于给外部传感器及内部的 ADC 供电，外接 0.1uF 电容到 VSS
13	VDD	电源
14	PB65/AI7/SEG31/Touch0/INT0/ LVDIN0	数字 IO，复用 ADC 输入 AI7，复用 SEG31，复用触摸按键 0，复用外部中断 0， 复用外部电压检测通道 0
15	PB66/AI8/SEG30/Touch1/INT1/ LVDIN1	数字 IO，复用 ADC 输入 AI8，复用 SEG30，复用触摸按键 1，复用外部中断 1， 复用外部电压检测通道 1
16	PB67/AI9/SEG29/PWM1/IR	数字 IO，复用 ADC 输入 AI9，复用 SEG29，复用 TimerB 的 PWM 输出，复用红 外载波输出
17	PB50/SEG28/Touch3/INT2/PW M2/CCP	数字 IO，复用 SEG28，复用触摸按键 3，复用外部中断 2，复用 TimerB 的 PWM 反向输出，复用 TimerC 捕捉输入
18	PB51/SEG27/Touch4/INT3/CCP	数字 IO，复用 SEG27，复用触摸按键 4，复用外部中断 3，复用捕捉输入
19	PA00	GPIO 0
20	PA02	GPIO 2
21	PA03	GPIO 3
22	PA07	GPIO 7
23	PA09	GPIO 9
24	GND	
25	PA10	GPIO 10
26	PA11/AIO_0	GPIO 11/ADC input 0
27	PA14/AIO_3	GPIO 14/ADC input 3
28	VDD_LDO	Internal LDO power supply/DCDC feedback
29	DCDC_SW	DCDC output
30	VDD3	3.3V power supply
Pin	Pin name	Description

31	PA15/AIO_4	GPIO 15/ADC input 4/ micbias output
32	XTAL16M_I	16MHz crystal input
33	XTAL16M_O	16MHz crystal output
34	XTAL32K_I	32.768KHz crystal input
35	XTAL32K_O	32.768KHz crystal output
36	PA18/AIO_7	GPIO 18/ADC input 7/ PGA negative input
37	P20/AIO_9	GPIO 20/ADC input 9/ PGA positive input
38	RST_N	reset, active low
39	VDD_RF	power supply decoupling for RF transceiver
40	RF	RF antenna
41	PA23/AIO_1	GPIO 23/ADC input 1/micbias reference
42	PB54/SEG24/SCL/INT3/PWM3	数字 IO，复用 SEG24，复用 I2C 的 SCL，复用外部中断 3，复用 TimerC 的 PWM 输出
43	PB55/SEG23/SDA/PWM4	数字 IO，复用 SEG23，复用 I2C 的 SDA，复用 TimerC 的 PWM 反向输出
44	PB56/SEG22/XOUT/SCK	数字 IO，复用 SEG22，复用低频晶振 XOUT，复用 SPI 的 SCK
45	PB57/SEG21/XIN/SDI/SDIO	数字 IO，复用 SEG21，复用低频晶振 XIN，复用 SPI 的 SDI 或 SDIO
46	PB10/SEG20/LEDC0/SDO/INT2	数字 IO，复用 SEG20，复用 LEDC0，复用外部中断 2，复用 SPI 的 SDO
47	PB11/SEG19/LEDC1	数字 IO，复用 SEG19，复用 LEDC1
48	PB12/SEG18/LEDC2	数字 IO，复用 SEG18，复用 LEDC2
49	PB13/SEG17/LEDC3/PWM3	数字 IO，复用 SEG17，复用 LEDC3，复用 TimerC 的 PWM 输出
50	PB14/SEG16/LEDC4/PWM4/CCP	数字 IO，复用 SEG16，复用 LEDC4，复用 TimerC 的 PWM 反向输出，复用 TimerB 捕捉输入
51	PB15/SEG15/LEDC5	数字 IO，复用 SEG15，复用 LEDC5
52	PB16/SEG14/LEDC6	数字 IO，复用 SEG14，复用 LEDC6
53	PB17/SEG13/LEDC7	数字 IO，复用 SEG13，复用 LEDC7
54	PB27/SEG12/LEDS7/TXD/SDA	数字 IO，复用 SEG12，复用 LEDS7，复用 UART 的数据发送端 TXD，复用 I2C 的 SDA
55	PB26/SEG11/LEDS6/RXD/SCL/INT2	数字 IO，复用 SEG11，复用 LEDS6，复用 UART 的数据发送端 RXD，复用 I2C 的 SCL，复用外部中断 2
56	PB25/SEG10/LEDS5	数字 IO，复用 SEG10，复用 LEDS5
57	PB24/SEG9/LEDS4	数字 IO，复用 SEG9，复用 LEDS4
58	PB23/SEG8/LEDS3	数字 IO，复用 SEG8，复用 LEDS3
59	PB22/SEG7/LEDS2	数字 IO，复用 SEG7，复用 LEDS2
60	PB21/SEG6/LEDS1	数字 IO，复用 SEG6，复用 LEDS1
61	PB20/SEG5/LEDS0	数字 IO，复用 SEG5，复用 LEDS0
Pin	**Pin name**	**Description**
62	PB37/SEG4	数字 IO，复用 SEG4
63	PB36/SEG3	数字 IO，复用 SEG3

64	PB35/SEG2	数字 IO，复用 SEG2

Note： All gpio support 1M/150kΩ pull up, 150kΩ pull down.

*: P33、P32、P31 和 P30 为一组 OTP 烧录引脚，分别对应 SCK、SDI、SDO 和 CLK。

Table 1: Pin functions of ST17H69 QFN64 package

3 System Block

The system block diagram of ST17H69 is shown in **Figure 1**.

3.1 CPU

The ST17H69 has an ARM Cortex-M0 CPU. The CPU, memories, and all peripherals are connected by AMBA bus fabrics.

The CPU will play controller role in BLE modem and run all user applications.

3.1.1 ARM M0

The ARM® Cortex™-M0 CPU has a 16-bit instruction set with 32-bit extensions (Thumb-2® technology) that delivers high-density code with a small-memory-footprint. By using a single-cycle 32-bit multiplier, a 3-stage pipeline and a Nested Vector Interrupt Controller (NVIC), the ARM Cortex™-M0 CPU makes program execution simple and highly efficient.

The main features of ARM® Cortex™-M0 CPU are listed below.

- Up to 96Mhz ARM Cortex™-M0 processor core.
    - Low gate count and high energy efficient.
    - ARMv6M architecture, Thumb ISA but no ARM ISA.
    - No cache and no TCM.
    - Up to 32 interrupts embedded NVIC.
    - SysTick timer.
    - Sleep/deep sleep mode.
    - Support low power WFI and WFE.
- Tight integration of system peripherals reduces area and development costs
- Thumb instruction set combines high code density with 32-bit performance
- power control optimization of system components
- Integrated sleep modes for low power consumption
- Fast code execution permits slower processor clock or increases sleep mode time
- Hardware multiplier
- Deterministic, high-performance interrupt handling for time-critical applications
- Serial Wire Debug reduces the number of pins required for debugging.
- APB interface to/from BLE modem.
- Dynamic and static clock gating to save power.
- No TRACE.

Some of these features are shared with the AP subsystem.

3.2 Memory

ST17H69 has total 96KB ROM, 64KB SRAM, 128KB-8MB FLASH and 256bit efuse. The physical address space of these memories is shown in **Figure 3**.

Prime Memory Space

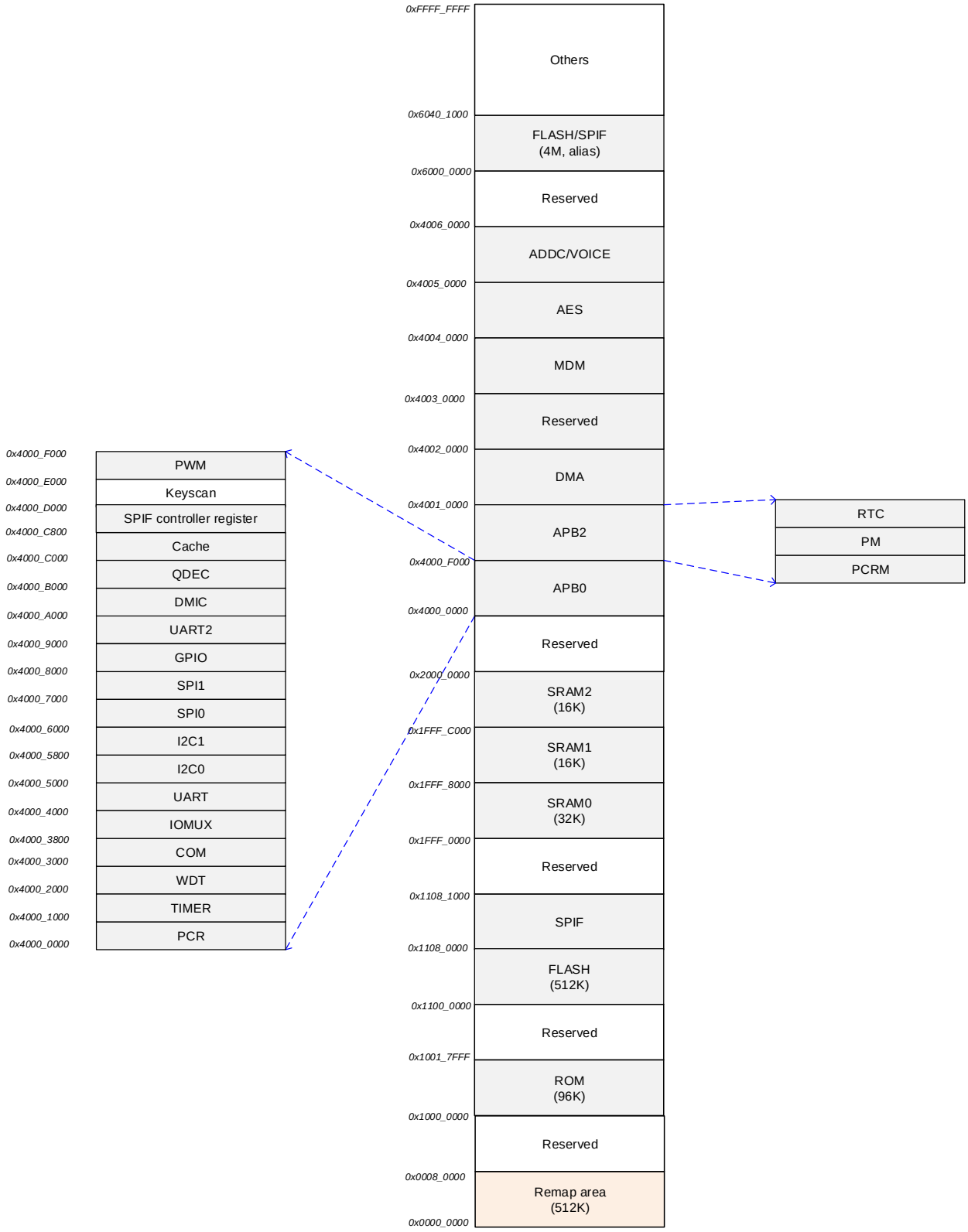

Figure 3: ST17H69 memory space

3.2.1 ROM

ST17H69 has 1 ROM.

	SIZE	CONTENT
ROM	96KB	Boot ROM. Protocol stack. Common peripheral drivers. ATE AT command.

Table 2: List of ROM

3.2.2 SRAM

ST17H69 has 5 SRAM blocks. All 5 SRAM blocks have retention capability, which can be configured individually. Normal operating voltage is 1.2V, and the voltage is adjustable at retention. All SRAM blocks can be used to store program or data.

	SIZE	CONTENT
SRAM0	32KB	
SRAM1	16KB	
SRAM2	16KB	
SRAM_BB	4KB	
SRAM_cache	8KB	

Table 3: List of SRAMs

3.2.3 FLASH

The size of FLASH can be 128KB to 8MB. Supports single-wire, 2-wire, and 4-wire reading, 2 wire reading mode by default. For FLASH greater than 4MB, supporting indirect addressing is needed.

3.2.4 eFuse

ST17H69 integrates 256bits internal nonvolatile one-time programmable EFUSE storage. With a serial interface, 1-bit can be programmed at one clock in program mode and 1-bit can be read at one time in read mode.

3.2.5 Memory Address Mapping

Name	Size（KB）	Master	Physical Address
ROM	96	M0	1000_0000~1001_7FFF
RAM0	32	M0	1FFF_0000~1FFF_7FFF
RAM1	16	M0	1FFF_8000~1FFF_CFFF
RAM2	16	M0	1FFF_D000~1FFF_FFFF
FLASH	512	M0	1100_0000~1107_FFFF 6000_0000~603F_FFFF

Table 4: Memory address mapping

3.3 Boot and Execution Modes

Only in CP Chip form, the chip enters CP boot mode after power on. ROM1 is then aliased to the 0x0 address and the chip program starts from ROM1.

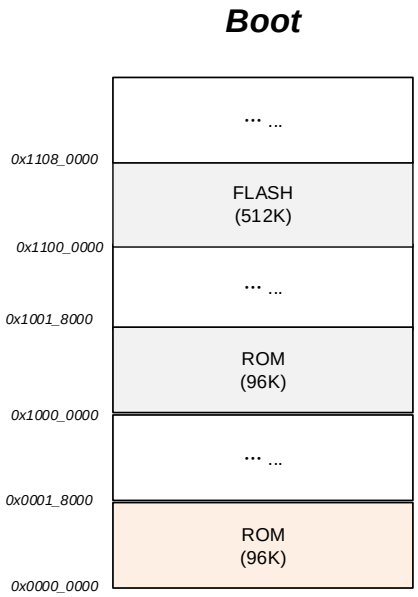

Figure 4: ST17H69 boot mode

3.3.1 Boot Loader

The boot loader in the ROM has the basic structure as shown below. The content in the FLASH should be specifically defined to allow boot loader to identify whether the FLASH content is valid, as shown in the example below. If the FLASH is valid, the ROM boot loader will put the chip in the normal mode and start normal program execution. If the FLASH is not valid, the boot loader will enter FLASH programming mode.

Address	Variable	Content
0	PRODUCT_MODE	Identify the chip mode
4	CODE_BASE	The base address of the code
8	CODE_LEN	The length of the code
C	BOOT_MODE	Identify mirror or FLASH mode

Table 5: Flash content example

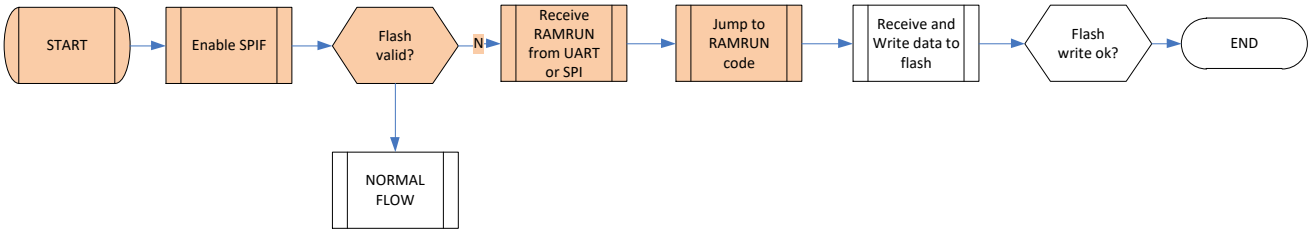

Figure 5: Bootloader flow

3.4 Power, Clock and Reset (PCR)

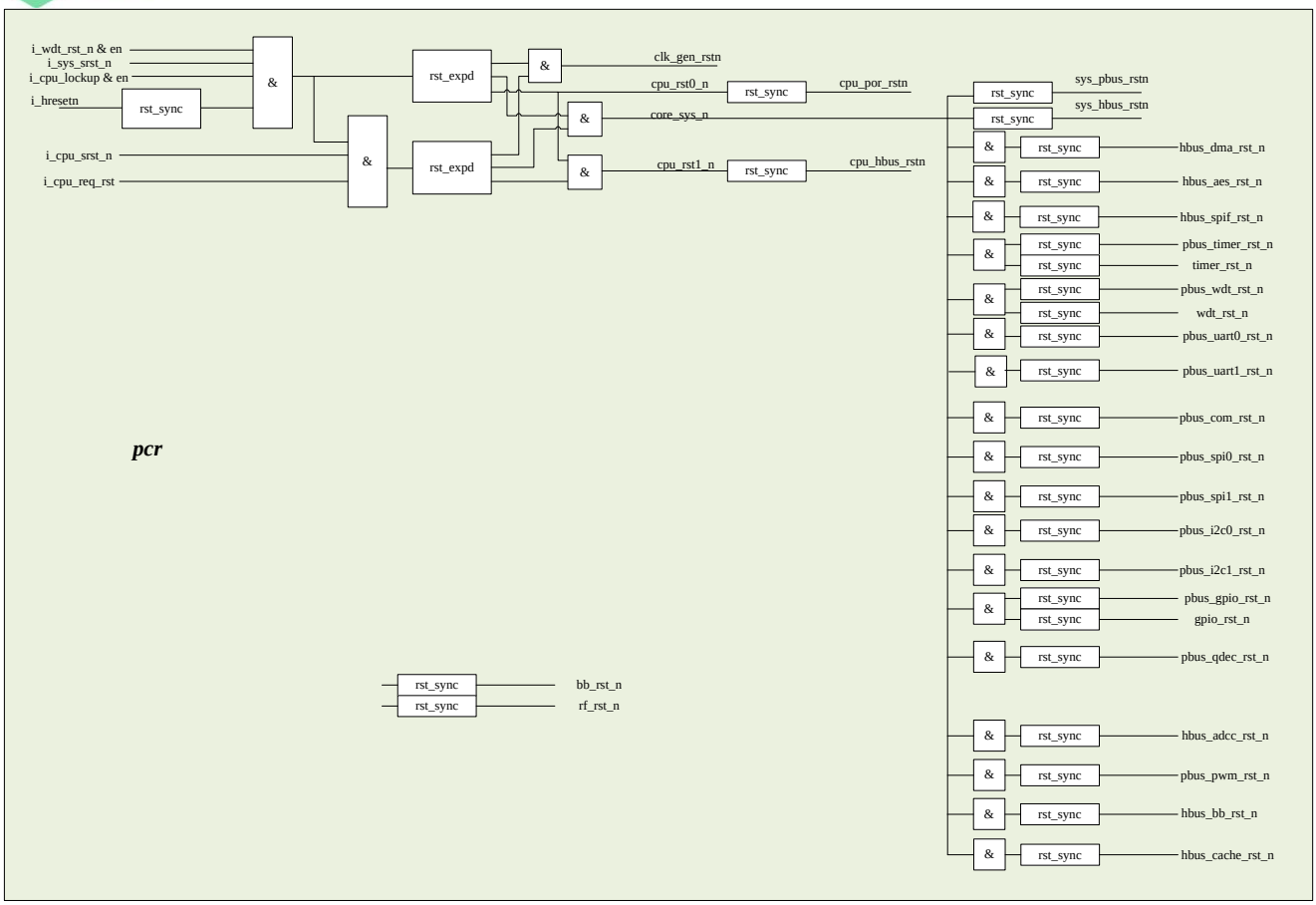

Figure 6: ST17H69 power, clock and reset

3.5 Power Management (POWER)

The power management system is highly flexible with functional blocks such as the CPU, radio transceiver, and peripherals saving separate power state control in addition to the System Sleep mode and OFF modes. When in System Normal mode, all functional blocks will independently be turned on depending on needed application functionality.

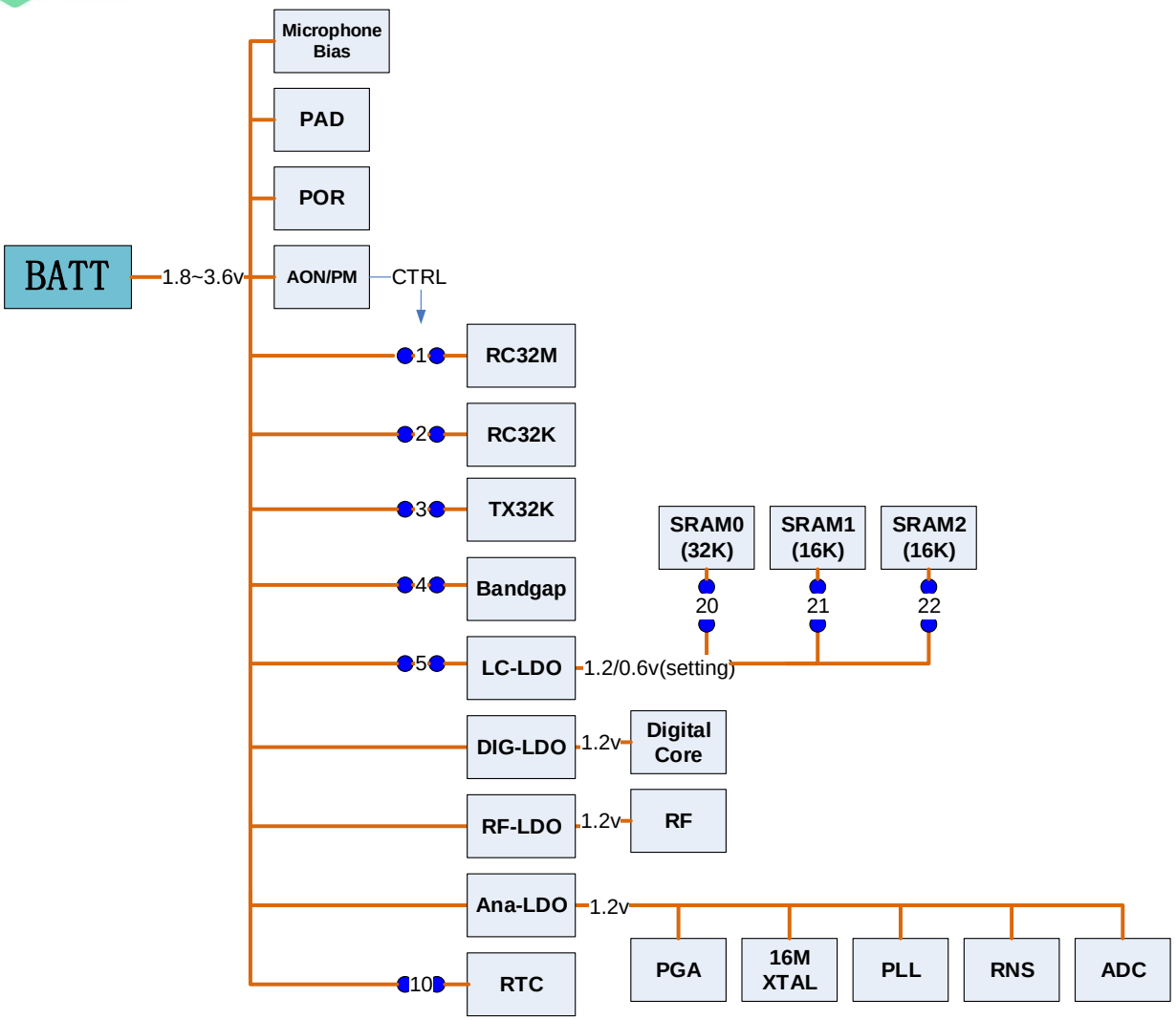

Figure 7: Power system

The following diagram is Normal, Sleep and Off mode. Switches are optional depending on user's request.

Switch	Normal	Sleep	Off
1RC32M	On	Off	Off
2RC32K	On	Optional	Off
3XT32K	On	Optional	Off
4bandgap	On	Off	Off
5LC-LDO	On	On	Off
10RTC	On	Optional	Off
20SRAM-32K	1.2v	0.6v	0
21SRAM-16K	1.2v	0.6v	0
22SRAM-16K	1.2v	0.6v	0

Table 6: Flash Switches of different power modes

3.6 Low Power Features

3.6.1 Operation and Sleep States

3.6.1.1 Normal State

3.6.1.2 Clock Gate State

The CPU executes WFI/WFE to enter clock gate state. After wake-up from clock-gate state, the CPU continues to execute the program from where it stopped. The wake-up sources includes interrupts and events. The wake-up sources are configured by the software according to applications.

3.6.1.3 System Sleep State

The wake-up sources include:

- IO
- RTC
- RESET
- UVLO reset

3.6.1.4 System Off State

The wake-up sources include：

- IOs
- RESET
- UVLO reset

3.6.1.5 UVLO

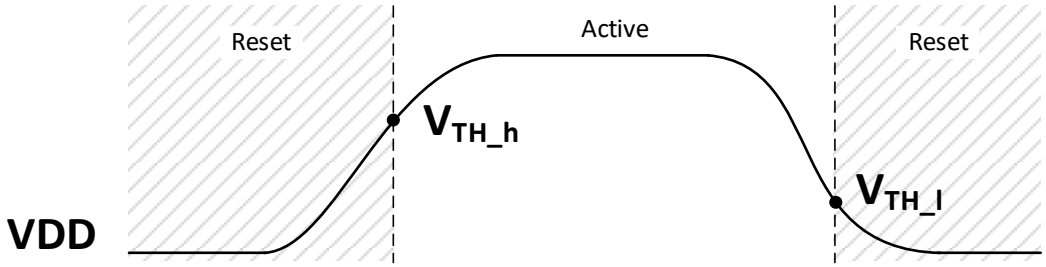

Figure 8: UVLO reset

VDD > VTH_h, release reset; VDD < VTH_l, enter reset.

VDD	Min.	TYP	Max.	Unit
V_{TH_h}	1.7	1.74	1.78	V
V_{TH_l}	1.63	1.66	1.69	V

Table 7: UVLO

3.6.2 State Transition

3.6.2.1 Entering Clock Gate State and Wake-up

CPU executes WFI/WFE.

3.6.2.2 Entering Sleep/off States and Wake-up

The PM registers identify whether the CPU is in mirror mode or FLASH mode before sleep or off, and record the remap and vectors. The CPU configures the corresponding PM registers to put the chip into sleep mode. After wake-up, the chip enters boot mode to execute boot code in the ROM. The ROM code checks the mode before sleep/off and the remap information, perform corresponding configurations, and starts to execute the program.

3.7 Interrupts

Interrupt Name	M0 Interrupt Number
	0
M0(coretime irq)	1
	2
	3
bb_irq	4
kscan_irq	5
rtc_irq	6
cpcom_ap_ipc_irq	7
apcom_ap_ipc_irq	8
	9
wdt_irq	10
uart0_irq	11
i2c0_irq	12
i2c1_irq	13
spi0_irq	14
spi1_irq	15
gpio_irq	16
uart1_irq	17
spif_irq	18
dmac_intr	19
timer_irq[1]	20
timer_irq[2]	21
timer_irq[3]	22
timer_irq[4]	23
timer_irq[5]	24
timer_irq[6]	25
	26
	27
Interrupt Name	**M0 Interrupt Number**
aes_irq	28
adcc_irq	29
qdec_irq	30
	31

Table 8: Interrupts

3.8 Clock Management

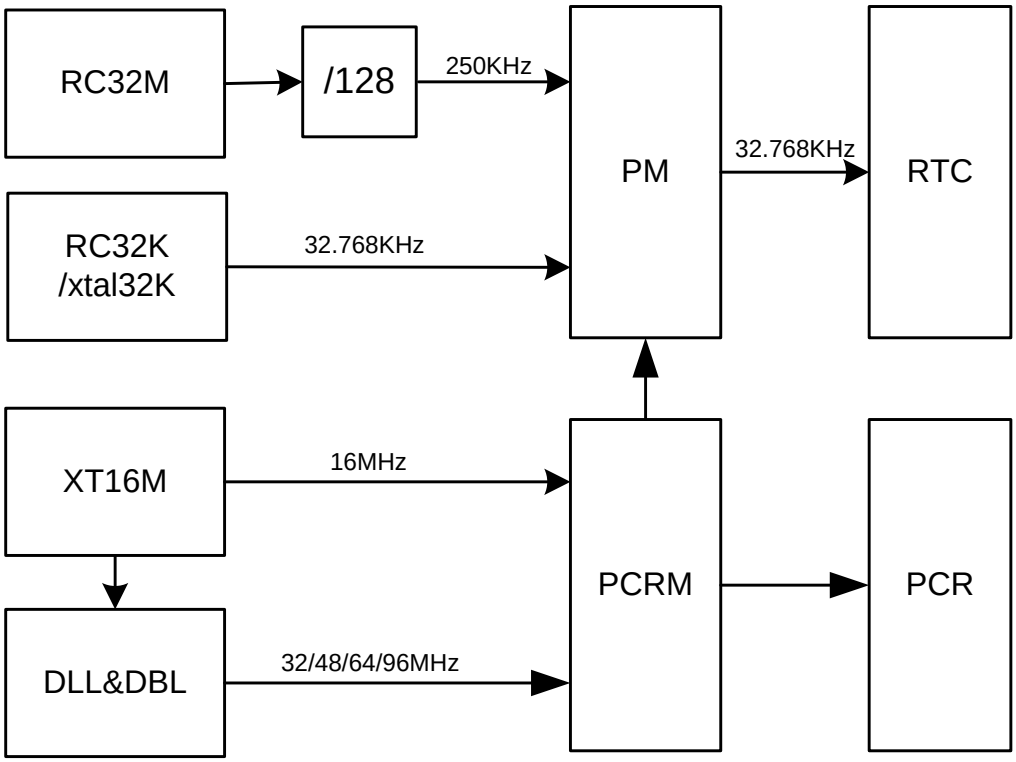

Figure 9: Clock management

There are two crystal clock sources: 16MHz crystal oscillator (XT16M) and 32.768kHz crystal oscillator (XT32k), of which the 32.768k crystal oscillator is optional. There are also two on chip RC oscillators: 32MHz RC oscillator (RC32M) and 32kHz RC oscillator (RC32k), both of which can be calibrated with respect to 16MHz crystal oscillator. If 32.768kHz crystal is not installed, RC32k oscillator would be periodically calibrated and used for RTC. At initial power up or wake up before XT16M oscillator starts up, RC32M is used as the main clock. An on-chip DLL generates higher frequency clocks such as 32/48/64/96MHz.

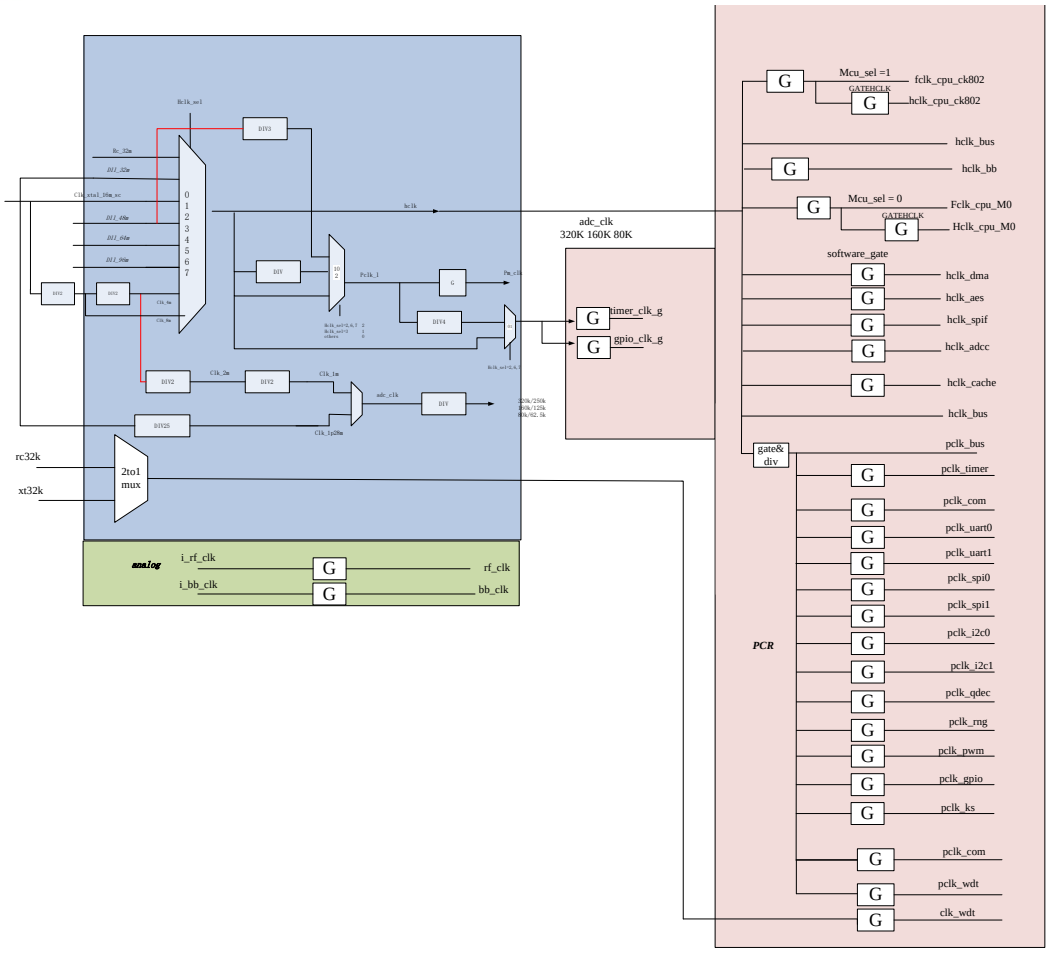

Figure 10: Clock structure diagram

3.9 IOMUX

The IOMUX provides a flexible I/O configuration, as the ports of most of the peripherals can be configured and mapped to any of the physical I/O pads (I/O at die boundary). These peripheral modules include I2C 0-1, UART0-1, PWM 0-5, SPI 0-1, Quadrature Decoder etc. However for other specific purpose peripherals, their IOs mappings are fixed when they are enabled. These specific purpose peripherals include JTAG, analog_ios, GPIOs and key scan.

Figure 11 below shows the IOMUX functional diagram.

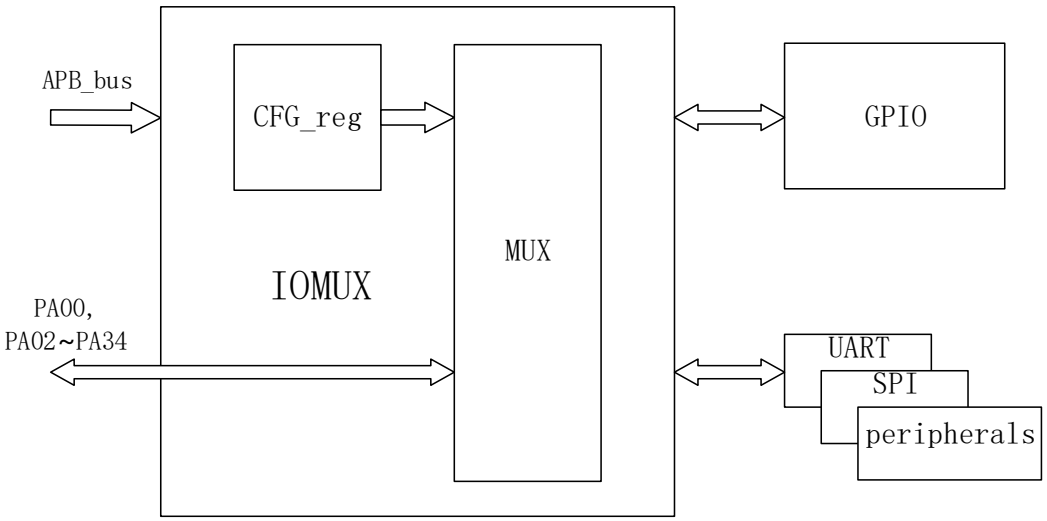

Figure 11: IOMUX structure diagram

There are 34 configurable pads which are from PA00 to PA07 and from PA09 to PA34. PA08 pad is assigned for TM pin which is a test mode pin. The table blow shows the mapping of the peripheral IOs that can be mapped through IOMUX. These include I2C 0-1, UART 0-1, PWM 0-5, SPI 0-1, Quadrature Decoder, 1.28MHz clock and dmic_out.

On the other hand, there are also special purpose peripherals, whose IOs are fixed to certain physical pads, when these peripheral functions are enabled. These special purpose peripherals include: JTAG, analog I/Os (ADC inputs), GPIO, and key scan. When they are enabled, their IOs are mapped to physical pads according to the following table.

#				Name
0	GPIO_PA00	GPIO		mk_in[0]
1	GPIO_PA01	GPIO		mk_out[0]
2	GPIO_PA02	SDW_IO		mk_in[1]
3	GPIO_PA03	SDW_CLK		mk_out[1]
4	GPIO_PA07	GPIO		mk_in[10]
5	TEST_MODE			
6	GPIO_PA09	GPIO		mk_out[4]
7	GPIO_PA10	GPIO		mk_in[4]
8	GPIO_PA11	GPIO	analog_io[0]	mk_out[11]
9	GPIO_PA14	GPIO	analog_io[3]	mk_out[2]
10	GPIO_PA15	GPIO	analog_io[4]	mk_in[2]
11	GPIO_PA16	XTALI(ANA)		mk_out[10]
12	GPIO_PA17	XTALO(ANA)		mk_out[9]
13	GPIO_PA18	GPIO	analog_io[7]	mk_in[5]
14	GPIO_PA20	GPIO	analog_io[9]	mk_out[5]
15	GPIO_PA23	GPIO	analog_io[1]	mk_in[6]
16	GPIO_PA24	GPIO	analog_io[2]	mk_out[3]
17	GPIO_PA25	GPIO	analog_io[8]	mk_in[3]
18	GPIO_PA26	GPIO		mk_out[8]
19	GPIO_PA27	GPIO		mk_in[9]
#				**Name**
20	GPIO_PA31	GPIO		mk_out[7]

21	GPIO_PA32	GPIO	mk_in[7]
22	GPIO_PA33	GPIO	mk_out[6]
23	GPIO_PA34	GPIO	mk_in[8]

Table 9: Peripheral IO mapped through IOMUX (special purpose)

In the IOMUX table above, the first column is the IO pad mapping in default mode, when no IOMUX function is selected and no special purpose peripherals such as analog IO, GPIO<0:3>, key scan, are enabled. In this mode, pin<0:3> are used for JTAG.

When analog IOs are enabled, pins<11:15>, <18:20> are connected to internal analog IOs. More specifically, analog_io<0:4><9> are connected to ADC inputs, analog_io<7,8> are connected to PGA inputs.

In JTAG mode, data output for JTAG test mode is mapped to P00; data input for JTAG test mode is mapped to P01; mode control input for JTAG test mode is mapped to P02; clock input for JTAG test mode is mapped to P03.

3.10 GPIO

The GPIO function configuration is shown in the table below.

#	GPIO_PAxx	Default MODE	Default IN_OUT	IRQ	Wakeup	ANA_IO
0	GPIO_PA00	GPIO	IN	√	√	
1	GPIO_PA01	GPIO	IN	√	√	
2	GPIO_PA02	GPIO	OUT	√	√	
3	GPIO_PA03	GPIO	IN	√	√	
4	GPIO_PA07	GPIO	IN	√	√	
5	TEST_MODE					
6	GPIO_PA09	GPIO	IN	√	√	
7	GPIO_PA10	GPIO	IN	√	√	
8	GPIO_PA11	GPIO	IN	√	√	
9	GPIO_PA14	GPIO	IN	√	√	ADC_CH2P_P14
10	GPIO_PA15	GPIO	IN	√	√	ADC_CH3N_P15
11	GPIO_PA16	XTALI(ANA)	ANA		√	
12	GPIO_PA17	XTALO(ANA)	ANA		√	
13	GPIO_PA18	GPIO	IN	√	√	ADC_CH0P_P18
14	GPIO_PA20	GPIO	IN	√	√	ADC_CH3P_P20
15	GPIO_PA23	GPIO	IN	√	√	ADC_CH1P_P23
16	GPIO_PA24	GPIO	IN	√	√	ADC_CH2N_P24
17	GPIO_PA25	GPIO	IN	√	√	ADC_CH0N_P25
18	GPIO_PA26	GPIO	IN	√	√	
19	GPIO_PA27	GPIO	IN	√	√	
20	GPIO_PA31	GPIO	IN	√	√	

Table 10: ST17H69 GPIO_PAxx Application Notes

#	GPIO_PBxx	ANA/IO	Function
0	GPIO_PB34/SEG1*	IO	数字 IO，复用 SEG1
1	GPIO_PB33/COM3/SEG0/SCK*	IO	数字 IO，复用 COM3（1/4DUTY）或 SEG0（1/3DUTY），复用 SPI 接口 SCK

2	GPIO_PB32/COM2/SDI*	IO	数字 IO，复用 COM2，复用 SPI 的 SDI
3	GPIO_PB31/COM1/SDO*	IO	数字 IO，复用 COM1，复用 SPI 的 SDO:
4	GPIO_PB30/COM0*	IO	数字 IO，复用 COM0
5	GPIO_PB43/AI3/Touch2/INT2/LVDIN2	ANA/IO	数字 I/O，复用 ADC 输入 AI3，复用触摸按键 2，复用外部中断 2，复用外部电 压检测通道 2
6	GPIO_PB42/AI2	ANA/IO	数字 I/O，复用 ADC 输入 AI2
7	GPIO_PB65/AI7/SEG31/Touch0/INT0/LVDIN0	ANA/IO	数字 IO，复用 ADC 输入 AI7，复用 SEG31，复用触摸按键 0，复用外部中断 0，复用外部电压检测通道 0
8	GPIO_PB66/AI8/SEG30/Touch1/INT1/LVDIN1	ANA/IO	数字 IO，复用 ADC 输入 AI8，复用 SEG30，复用触摸按键 1，复用外部中断 1，复用外部电压检测通道 1
9	GPIO_PB67/AI9/SEG29/PWM1/IR	ANA/IO	数字 IO，复用 ADC 输入 AI9，复用 SEG29，复用 TimerB 的 PWM 输出，复用红外载波输出
10	GPIO_PB50/SEG28/Touch3/INT2/PWM2/CCP	IO	数字 IO，复用 SEG28，复用触摸按键 3，复用外部中断 2，复用 TimerB 的 PWM 反向输出，复用 TimerC 捕捉输入
11	GPIO_PB51/SEG27/Touch4/INT3/CCP	IO	数字 IO，复用 SEG27，复用触摸按键 4，复用外部中断 3，复用捕捉输入
12	GPIO_PB54/SEG24/SCL/INT3/PWM3	IO	数字 IO，复用 SEG24，复用 I2C 的 SCL，复用外部中断 3，复用 TimerC 的 PWM 输出
13	GPIO_PB55/SEG23/SDA/PWM4	IO	数字 IO，复用 SEG23，复用 I2C 的 SDA，复用 TimerC 的 PWM 反向输出
14	GPIO_PB56/SEG22/XOUT/SCK	ANA/IO	数字 IO，复用 SEG22，复用低频晶振 XOUT，复用 SPI 的 SCK
15	GPIO_PB57/SEG21/XIN/SDI/SDIO	ANA/IO	数字 IO，复用 SEG21，复用低频晶振 XIN，复用 SPI 的 SDI 或 SDIO
16	GPIO_PB10/SEG20/LEDC0/SDO/INT2	IO	数字 IO，复用 SEG20，复用 LEDC0，复用外部中断 2，复用 SPI 的 SDO
17	GPIO_PB11/SEG19/LEDC1	IO	数字 IO，复用 SEG19，复用 LEDC1
18	GPIO_PB12/SEG18/LEDC2	IO	数字 IO，复用 SEG18，复用 LEDC2
19	GPIO_PB13/SEG17/LEDC3/PWM3	IO	数字 IO，复用 SEG17，复用 LEDC3，复用 TimerC 的 PWM 输出
20	GPIO_PB14/SEG16/LEDC4/PWM4/CCP	IO	数字 IO，复用 SEG16，复用 LEDC4，复用 TimerC 的 PWM 反向输出，复用 TimerB 捕捉输入
21	GPIO_PB15/SEG15/LEDC5	IO	数字 IO，复用 SEG15，复用 LEDC5
22	GPIO_PB16/SEG14/LEDC6	IO	数字 IO，复用 SEG14，复用 LEDC6
23	GPIO_PB17/SEG13/LEDC7	IO	数字 IO，复用 SEG13，复用 LEDC7
#	**GPIO_PBxx**	**ANA/IO**	**Function**
24	GPIO_PB27/SEG12/LEDS7/TXD/SDA	IO	数字 IO，复用 SEG12，复用 LEDS7，复用 UART 的数据发送端 TXD，复用 I2C 的 SDA
25	GPIO_PB26/SEG11/LEDS6/RXD/SCL/IN	IO	数字 IO，复用 SEG11，复用 LEDS6，复用

	T2		UART 的数据发送端 RXD，复用 I2C 的 SCL，复用外部中断 2
26	GPIO_PB25/SEG10/LEDS5	IO	数字 IO，复用 SEG10，复用 LEDS5
27	GPIO_PB24/SEG9/LEDS4	IO	数字 IO，复用 SEG9，复用 LEDS4
28	GPIO_PB23/SEG8/LEDS3	IO	数字 IO，复用 SEG8，复用 LEDS3
29	GPIO_PB22/SEG7/LEDS2	IO	数字 IO，复用 SEG7，复用 LEDS2
30	GPIO_PB21/SEG6/LEDS1	IO	数字 IO，复用 SEG6，复用 LEDS1
31	GPIO_PB20/SEG5/LEDS0	IO	数字 IO，复用 SEG5，复用 LEDS0
32	GPIO_PB37/SEG4	IO	数字 IO，复用 SEG4
33	GPIO_PB36/SEG3	IO	数字 IO，复用 SEG3
34	GPIO_PB35/SEG2	IO	数字 IO，复用 SEG2

Table 11: ST17H69 GPIO_PBxx Application Notes

3.10.1 DC Characteristics

TA=25℃, VDD=3 V

PARAMETER	TEST CONDITIONS	Min.	TYP	Max.	Unit
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.4			V
Logic-0 input current	Input equals 0 V	-50		50	nA
Logic-1 input current	Input equals VDD	-50		50	nA
Logic-0 output voltage, 10-mA pins	Output load 10 mA			0.5	V
Logic-1 output voltage, 10-mA pins	Output load 10 mA	2.5			V

Table 12: DC Characteristics

4 Peripheral Blocks

4.1 2.4GHz Radio

The 2.4 GHz RF transceiver is designed to operate in the worldwide ISM frequency band at 2.4 to 2.4835 GHz. Radio modulation modes and configurable packet structure make the transceiver interoperable with Bluetooth LE 5.2 protocol implementations.

- General modulation format
    - FSK (configurable modulation index) with configurable Gaussian Filter Shaping
    - OQPSK with half-sine shaping
    - On-air data rates
    - 125kbps/250kbps/500kbps/1Mbps/2Mbps
- Transmitter with programmable output power of -20dBm to +10dBm, in 3dB steps
- RSSI function (1 dB resolution, ± 2 dB accuracy)
- Receiver sensitivity
    - -105dBm@125Kbps GFSK
    - -100dBm@500Kbps GFSK
    - -99dBm@1Mbps BLE
    - -96dBm@2Mbps BLE
    - -103dBm@ 250Kbps Zigbee 3.0
- Embedded RF balun
- Integrated frac-N synthesizer with phase modulation

4.2 Timer/Counters (TIMER)

The implementation can include a 32-bit SysTick system timer, that extends the functionality of both the processor and the NVIC. When present, the NVIC part of the extension provides:

- A 32-bit system timer (SysTick)
- Additional configurable priority SysTick interrupt.

General purpose timers are included in the design. This timer is Synopsys DW_apb_timer. With the input clock running at 4Mhz.

4.3 Real Time Counter (RTC)

The Real Time Counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK). The RTC features a 24 bit COUNTER, 12 bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

4.4 AES-ECB Encryption (ECB)

The ECB encryption block supports 128 bit AES encryption. It can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption.

4.5 Watchdog Timer (WDT)

A count down watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up. The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU.

4.6 SPI (SPI0, SPI1 Two Independent Instances)

The SPI interface supports 3 serial synchronous protocols which are SPI, SSP and Microwire serial protocols. SPI wrapper contains one SPI master and one SPI slave. They are logically exclusive. Only one block is alive at a time. The operation mode for master mode and slave mode is controlled by PERI_MASTER_SELECT Register in COM block.

bit	Reset value	Definition
1	0	SPI1 is master mode when set
0	0	SPI0 is master mode when set

Table 13: PERI_MASTER_SELECT Register bit definition (base address = 0x4000_302C)

4.7 I2C (I2c0, I2c1 Two Independent Instances)

This I2C block support 100Khz, and 400Khz modes. It also supports 7-bit address and 10-bit address. It has built-in configurable spike suppression function for both lines.

4.8 UART (UART0, UART1 Two Independent Instances)

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in HW up to 1Mbps baud. Parity checking and generation for the 9th data bit are supported.

The GPIOs used for each UART interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pin out and enables efficient use of board space and signal routing.

4.9 DMIC/AMIC Data Path

The voice in interface supports one analog MIC (SAR-ADC) and two digital MIC (L+R), different output sample rate (64KHz, 32KHz, 16KHz and 8KHz), and different voice compress algorithm. For the Digital MIC, PDM signal is sampled at 1.28MHz(4x320KHz). L channel is sampled at raising edge, R channel is sampled at falling edge. For PCM-LOG and CVDS, output data rate is 64Kbps (8KHz x 8bit).

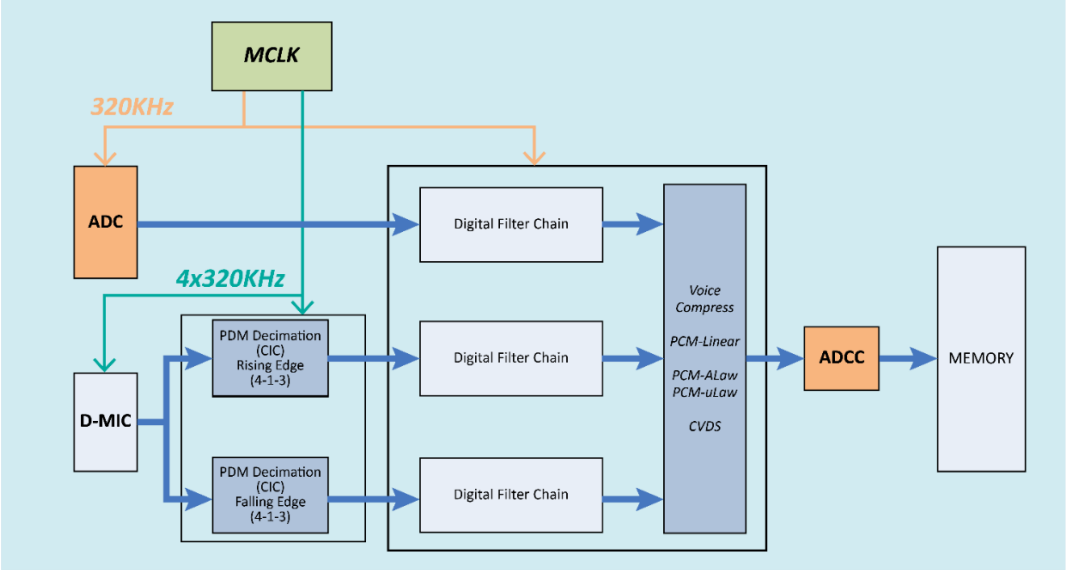

Figure 12: Block Diagram of Voice In Interface

Base address: 0x4005_0000

OFFSET	TYPE	RESET	NAME	DESCRIPTION
0x00			**ADCC voice enable**	
[31:1]	—	31'b0	reserved	
[0]	RW	1'b0	Enable	Setting this bit to “1” will enable voice core work
0x08			**ADCC reserved reg**	
[31:0]	—	32'b0	reserved	
0x0C			**ADCC voice control 1**	
[31:23]	—	9'd0	reserved	
[22:16]	RW	7'd40	gain_ctrl	Vocie Process Gain control,+-20dB, Step is 0.5dB. Voice_gain = (gain_ctrl-40)*0.5dB gain_ctrl with in[0 80]
[15:14]	—	2'd0	reserved	
[13:12]	RW	2'd2	encode_mode	Voice compress encode mode sel: 0:pcm a-law 1:pcm u-law 2:cvsd 3:bypass
[11:10]	—	2'd0	reserved	
[9:8]	RW	2'd0	voice_sel	Voice Process Output Rate Sel: 0:64Ksps 1:32Ksps 2:16Ksps 3:8Ksps
[7]	RW	1'b0	fir filter bandwidth	1:4K,0:8K
[6]	RW	1'b0	pcm_au_sel	pcm encode，1:a-law 0：u-law
[5]	RW	1'b0	lr_sel	
[4]	—	1'b0	reserved	
0x0C			**ADCC voice control 1**	
[3:2]	RW	2'd1	notch_bw	Dc Notch Filter BW

				0:bypass the DC Notch filter Other: one order high pass iir filter 1:a(n)+a(n-1)* (1-1/2^14) 2:a(n)+a(n-1)* (1-2/2^14) 3:a(n)+a(n-1)* (1-3/2^14)
[1]	RW	1'b0	plry_sel	Adc input polarity selection 0:voiceIn-2048 1:2048-voiceIn
[0]	RW	1'b0	mic_sel	DMIC and AMIC selection: 0:AMIC 1:DMIC
0x10			**ADCC voice control 2**	
[31]	—	1'd0	Reserved	
[30:20]	RW	11'd64	gain_max	Max Gain in auto mute process
[19:16]	—	4'd6	gain_maxbw	Max Gain BW in auto mute process
[15:14]	RW	2'd0	reserved	
[13:8]	RW	6'd9	amut_gdut	Auto mute adjust duration
[7:4]	RW	4'd0	amut_gst2	Auto mute gain increasingstep
[3:0]	RW	4'd1	amut_gst1	Auto mute gain increasingstep
0x14			**ADCC voice control 3**	
[31]	—	1'b0	Reserved	
[30:20]	RW	11'd55	amut_lvl2	Auto Mute Stop Level
[19]	—	1'b0	reserved	
[18:8]	RW	11'd10	amut_lvl1	Auto Mute Start Level
[7:1]	—	7'b0	reserved	
[0]	RW	1'b0	amut_byps	Bypass automate function
0x18			**ADCC voice control 4**	
[31:16]	—	16'd0	Reserved	
[15:8]	RW	8'd48	amut_alvl	Adaptive Mute Level control: 0: disable adaptive Mute level Other: Mute level1 = adpPower+amut_lvl1 Mute level2 = adpPower+amut_lvl2 adpPower is estimated over (amut_alv1<<amut_win1) samples
[7]	—	1'd0	reserved	
[6:4]	RW	3'd3	amut_beta	Voice Level Estimation filter bandwidth(one order low pss iir filter):
[3:0]	RW	4'd10	amut_winl	Voice Level estimation window length: samples = 1<<amut_winl

Table 14: ADCC Voice

4.9.1 Filter Chain Design

For D-MIC input, PDM Decimation (CIC) will convert the 1-bit PDM signal to 12 bit PCM signal. And the sample rate will be converted from 1.28MHz to 320KHz. The output data of the PDM Decimation will

be connected to the Digital Filter chain.

For the A-MIC input, SAR-ADC will convert the signal to 12bit 320KHz digital samples. The Digital Filter chain will process the data same as the D-MIC path.

The Output sample rate of the Digital filter chain is programmable. 64KHz, 32KHz, 16KHz, 8KHz. The maximum value of the sample's bit-width is 16bit.

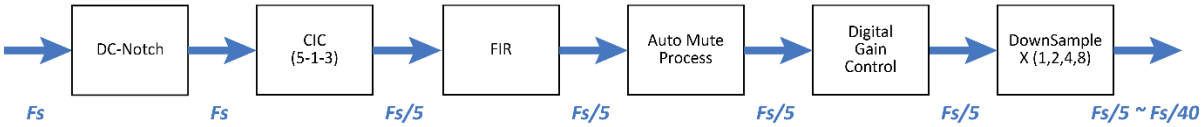

Figure 13: Digital Filter Chain

4.9.2 Auto Mute Process

Signal Level Estimate will check the input signal level with configurable window size. Mute threshold can be updated according to the signal level estimation or being configured by the register. There are two thresholds, one for MUTE_ON, another for MUTE_OFF. Gain step of MUTE_ON and MUTE_OFF can be configured individually.

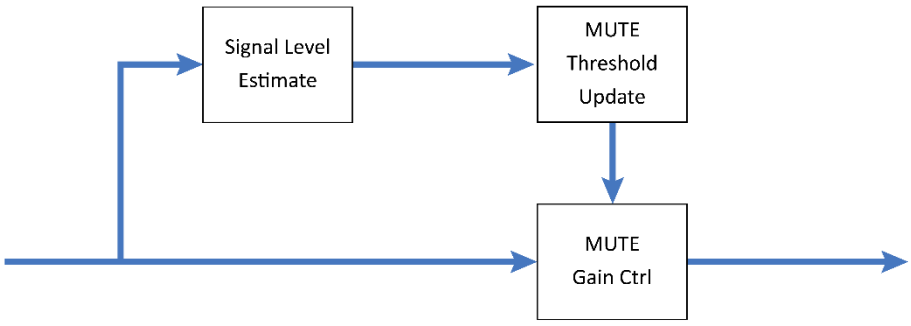

Figure 14: Auto Mute Process

4.9.3 Digital Gain Control

Digital gain is implemented by one Look up table. The gain error has been controled within 0.05dB.

4.9.4 Voice Compression

PCM-LOG support u-Law and a-Law. According to the ITU-G711 standard. The input data is 13~14bit @ 8KHz. The output data is 8bit @ 8KHz, 64Kbps. Also, it support 64Kbps CVSD according to the BT standard. Its Input is 16bit @64KHz, and its output is 1bit @ 64KHz. PCM-Linear is for the raw data without compression.

4.10 Pulse Width Modulation (PWM)

ST17H69 supports 6 channels of Pulse Width Modulation (PWM) outputs. PWM outputs generate waveforms with variable duty cycle or pulse width programmed by registers. And each of the 6 PWM outputs can be individually programmed. Their duty cycles are controlled by programming individual

counters associated with each channel.

The master clock is 16MHz. For each PWM outputs, first there is a prescaler (pre-divider) with division ratio of 2 to 128 (only 2^N division ratios are supported), followed by another 16bit counter with programmable max count, denoted as top_count. When the 16bit counter counts from 0 to top_count, it resets back to 0. So the frequency of the PWM is given by:

Freq_PWM = 16MHz / (N_prescaler * N_top_count);

A threshold counter number can be programmed, when the 16bit counter reaches the threshold, PWM output toggles. So the duty cycle is:

Duty_cycle_PWM = N_threshold/N_top_count;

The polarity of the PWM can also be programmed, which indicates output 1 or 0 when counter is below/above the threshold. A PWM waveform vs counter values are illustrated in the following **Figure 15**, where the polarity is positive. Also in this case the counter ramps up and then resets, we call it “up mode”.

There is also a “up and down mode”, where the counter ramps up to count_top and then ramps down, instead of reset.

As discussed above, the key register bits for one PWM channel are: 16bit top_count, 16bit threshold count, 3bit prescaler count, PWM polarity, PWM mode (up or up/down), PWM enable, and PWM load enable (load new settings). All 6 PWM channels can be individually programmed by registers with addresses from 0x4000_E004 to 0x4000_E044. In addition, one should enable registers 0x4000_E000<0><4> to allow all PWM channels can be programmed.

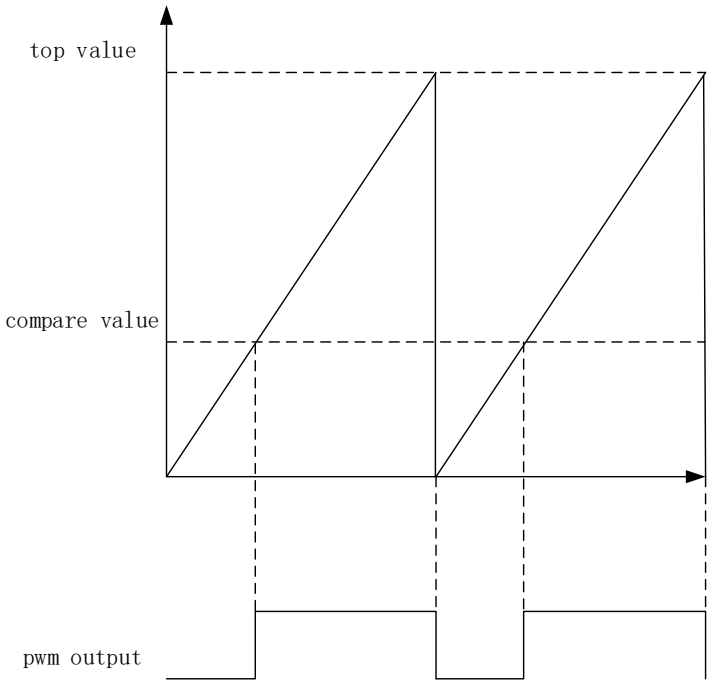

Figure 15: PWM operation

4.11 Quadrature Decoder (QDEC)

The quadrature decoder provides buffered decoding of quadrature-encoded sensor signals with input debounce filters. It is suitable for mechanical and optical sensors. The sample period and accumulation are configurable to match application requirements. The quadrature decoder has three-axis capability and index channel support. It can be programmed as 4x/2x/1x count mode.

4.12 Key Scan (KSCAN)

Keyscan supports key matrix with upto 16 rows by 18 columns. Each individual rows or columns can be enabled or disabled through register settings. GPIO pins can be configured to be used for key scan. A few key scan Parameters can be set through registers, including polarity (low or high indicating key pressed); support multi-key-press or only single-key-press; de-bounce time (the time duration a key press is deemed valid) from 0 to 128mS with 255us step.

A valid key press can trigger an interrupt when keyscan interrupt is enabled. After a keyscan interrupt is serviced, writing 1 to the interrupt state register bit can clear the state bit.

The keyscan has a manual mode and an auto mode. For manual mode, when a keyscan interrupt is received, it is upo the MCU/software to scan the keyscan output pins and check the input pins, to determine which keys have been pressed. Manual mode is relatively slow and need CPU to process. On the contrary, in automode keyscan will automatically scan the output/input pins, and store the row/column info corresponding to the key pressed into read only registers, then trigger an interrupt for software to retrieve key press information.

4.13 Analog to Digital Converter (ADC) with Programmable Gain Amplifier (PGA)

The 12bit SAR ADC has total 10 inputs. Among them, there are two for PGA inputs, and two differential inputs for the on-chip temperature sensor. The other six inputs can be programmed to 4 pair differential inputs or six single-ended inputs. There is a manual mode with which the ADC can be configured to convert a specific input in single-ended or differential and with a specific ADC clock rate. There is also an auto sweep mode, namely all enabled input channels can be swept automatically in order by the ADC and the converted data will be stored at corresponding memory locations.

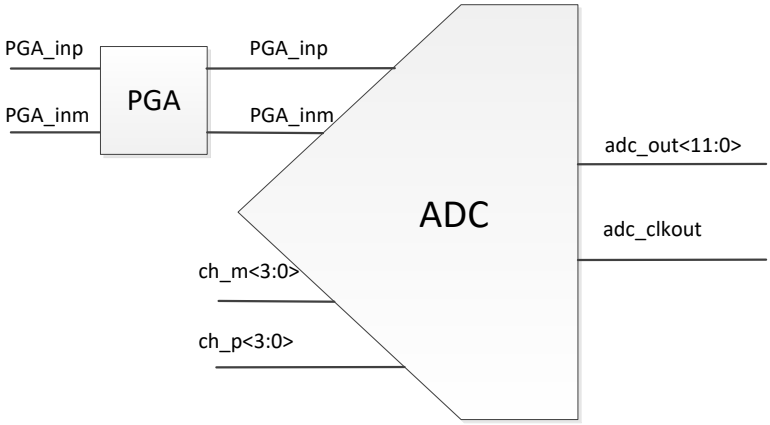

Figure 16: ADC

4.13.1 PGA Path

The PGA provides 42dB gain range from 0dB to 42dB in 3dB steps.

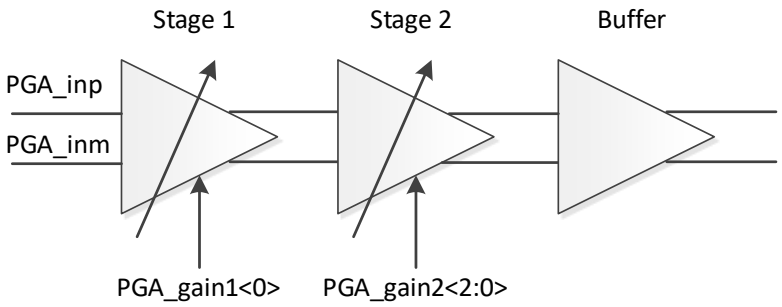

Figure 17: PGA path

pga_gain1<0>	Stage1 gain (v/v)	pga_gain2<2>	pga_gain2<1>	pga_gain2<0>	Stage2 gain (v/v)
0	5	0	0	0	37/4
1	15	0	0	1	36/5
		0	1	0	35/6
		0	1	1	34/7
		1	0	0	33/8
		1	0	1	32/9
		1	1	0	31/10
		1	1	1	30/11

Table 15: PGA gain

Set PGA_SEenable to “1”, PGA will be set to Single-ended mode by pulling the PGA into its Common-mode voltage.

4.13.2 ADC Path

By default the ADC is configured in manual mode. In this mode, the ADC clock rate can be configured to 80k/160k/320k sample per second. Select the pair of inputs and configure it to differential or singled-ended (positive or negative). By default it is differential. After enabling, the ADC will take samples with the configured clock rate and store the data to a channel dependent memory location. For each channel a memory size of 128Byte is allocated, when it is full an interrupt bit will be flagged. Each sample of 12bits takes 2 Byte memory space.

ADC can also be configured into auto channel sweep mode by setting the “adc_ctrl_override” bit to 0, with which the enabled channels will be sampled in the configured order automatically. The ten ADC input channels can be configured by programming their corresponding registers. Their configurations include sampling time, enable/disable, differential/single-ended, and continuous sampling/single-shot, based on the following register table. The sampled data is stored in the corresponding memory locations as in manual mode.

Base address: 0x4000_F000

0x6C	ADC_CTL0	Register Description
[31:16]	auto mode config temp sense, differntial inputs	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or

		one shot 1. For auto channel sweep mode only
[15:0]	auto mode config PGA inputs, differential inputs	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
0x70	**ADC_CTL1**	**Register Description**
[31:16]	auto mode config input A, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	auto mode config input A positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
0x74	**ADC_CTL2**	**Register Description**
[31:16]	auto mode config input B, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	auto mode config input B positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
0x78	**ADC_CTL3**	**Register Description**
[31:16]	auto mode config input C, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
0x78	**ADC_CTL3**	**Register Description**
[15:0]	auto mode config input C positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only

Table 16: ADC channel configurations

4.13.3 ADC Channel <3:0> Connectivity

ADC	Hardwired	Single	differential	note
aio<0>	gpio<11>	√	Input B negative	
aio<1>	gpio<23>	√	Input B positive	micphone bias reference voltage
aio<2>	gpio<24>	√	Input C negative	
aio<3>	gpio<14>	√	Input C positive	

aio<4>	gpio<15>	√	Input D negative	micphone bias
aio<5>	gpio<16>			32K XTAL input
aio<6>	gpio<17>			32K XTAL output
aio<7>	gpio<18>		Input A positive	pga in+
aio<8>	gpio<25>		Input A negative	
aio<9>	gpio<20>	√	Input D positive	pga in-

Table 17: ADC channel connectivity

Aio<9:7,4:0>can be selected through an analog Mux by programming aio_pass<7:0> and aio_attn<7:0>. For example, register 0x4000_F020<8><0> set to 01, then Aio<0> is connected to ADC input B negative.

0x4000_F020		Register Description
[15 : 8]	Attenuation ctrl	attn[7:0]. analogIO control for {aio<9>, aio<8>,aio<7>,aio<4>, aio<3>, aio<2>, aio<1>, aio<0>}. {attn[x], pass[x]}: 00 switch off 01 pass through 10 attenuate to 1/4 11 NC

0x4000_F020		Register Description
[7 : 0]	pass ctrl	pass[7:0]. analogIO control for {aio<9>, aio<8>,aio<7>,aio<4>, aio<3>, aio<2>, aio<1>, aio<0>}. {attn[x], pass[x]}: 00 switch off 01 pass through 10 attenuate to 1/4 11 NC note: analog IO sharing gpio<11>/aio<0> gpio<23>/aio<1>/micphone bias reference voltage gpio<24>/aio<2> gpio<14>/aio<3> gpio<15>/aio<4>/micphone bias gpio<16>/aio<5>/32K XTAL input gpio<17>/aio<6>/32K XTAL output gpio<18>/aio<7>/pga in+ gpio<25>/aio<8> gpio<20>/aio<9>/pga in-

Table 18: analog Mux

4.14 带 PGA 和 Buffer 功能的 Σ-Δ ADC

模数转换器（Σ-Δ ADC）24bits 分辨率，最高 ENOB 22.6bits，带有可编程增益放大器（PGA）和输入缓冲器（Buffer），其框图如下图所示。

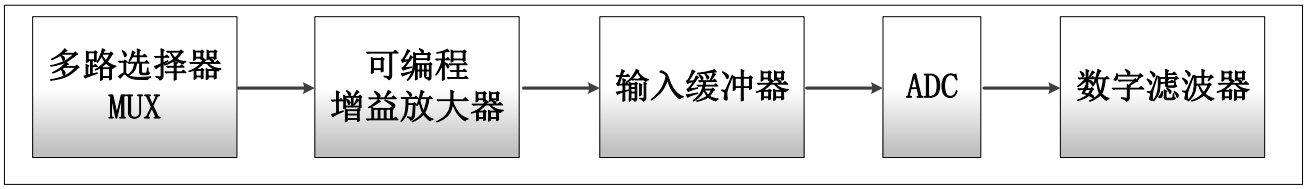

Figure 18: ADC blockdiagram

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x19B	ADCON1	MODG1	PGAGS[2:0]			LN	ADPS	ADCHOPEN	ADCEN
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	0	0	1	0
SynReset		u	u	u	u	u	u	u	u

Table 19: ADC Control Register 1

ADPS：ADC 电源选择

“0”，VSR，默认；“1”，VDD。

ADCEN：ADC 使能信号

“0”，关闭，默认；“1”，使能。

MODG1、PGAGS[2:0]、LN 和 ADCCHOPEN 的说明请参考**表 26 ADC Gain Configuration** 和**表 29 ADC Reference Voltage**。

待机或休眠之前，请将 ADCON1 寄存器清零。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1ED	SARDATAH	RFOS[1:0]		RFEN	RFSEL	写为 P65SREN 读为 sar_result[11]	写为 SARIN_SEL[2:0] 读为 sar_result[10:8]		
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	x	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 20: SARDATAH Register

SARDATAH 寄存器写操作时只能使用赋值语句操作。

RFOS[1:0]：检测干扰的阈值设置；

RFEN：检测干扰使能，1 为使能，默认为 0；

RFSEL：检测干扰的信号源，1 为检测 AI1，0 为检测 AI0。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1D	PT6SREN	P6SREN[7:6]		RFY	-	-	-	-	-
R/W		y		y	-	-	-	-	-
AsyReset		0		x	-	-	-	-	-
SynReset		u		u	-	-	-	-	-

Table 21: PT6SREN Register

RFY：AI0 或 AI1 受到干扰的标志

“1”AI0 或者 AI1 受到干扰；
“0”AI0 或者 AI1 信号正常。

4.14.1 ADC 的输入通道选择

多路选择器可以选择不同的输入通道，包括外部的模拟输入、内部的温度传感器和内部的基准信号等，由寄存器 AINSEL 来进行控制，具体可以参考**表 24 ADC Output Channels**。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x19E	AINSEL		ADIPS[3:0]			ADINS[3:0]			
R/W		y	y	y	y	y	y	y	y
AsyReset		0	1	0	1	0	1	0	1
SynReset		u	u	u	u	u	u	u	u

Table 22: AINSEL Register

ADIPS[3:0]：输入正端；
ADINS[3:0]：输入负端。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x19C	ADCON2	--	LVDIOEN[2:0]			AI3EN	AI2EN	AI1PD	AI0PD
R/W		--	y	y	y	y	y	y	y
AsyReset		--	0	0	0	1	1	0	0
SynReset		--	u	u	u	u	u	u	u

Table 23: ADC Control Register 2

AI3EN：AI3/P43 选择作为模拟端口还是数字端口
“1”模拟端口，默认
“0”数字端口
AI2EN：AI2/P42 选择作为模拟端口还是数字端口
“1”模拟端口，默认
“0”数字端口
AI1PD：AI1 下拉电阻使能
“1”下拉电阻使能
“0”下拉电阻关闭，默认
AI0PD：AI0 下拉电阻使能
“1”下拉电阻使能
“0”下拉电阻关闭，默认

ADIPS[3:0]	VINP	ADINS[3:0]	VINN
0000	VSR	0000	VSR
0001	AI0	0001	AI0
0010	AI1	0010	AI1
0011	AI2	0011	AI2
0100	AI3	0100	AI3
ADIPS[3:0]	**VINP**	**ADINS[3:0]**	**VINN**
0101 (Default)	ACM	0101 (Default)	ACM

0110	TSP (Temperature Sensor Positive output)	0110	TSP (Temperature Sensor Positive output)
0111	TSN (Temperature Sensor Negative output)	0111	TSN (Temperature Sensor Negative output)
1000	AI7	1000	AI7
1001	AI8	1001	AI8
1010	VSS	1010	VSS
1011	AI9	1011	AI9
1100~1111	Reserve	1100~1111	Reserve

Table 24: ADC Output Channels

4.14.2 ADC 的增益设置

增益也有多种选择，对应的增益、输入范围和输入阻抗等受可编程增益放大器和输入缓冲器影响，具体可以参考**表 26 ADC Gain Configuration**。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x192	VSRCON	MODG2	RD_TMB_SEL	RD_TMC_SEL	BGEN	VSREN	VSRS[2:0]		
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	1	0	1	0
SynReset		u	u	u	u	u	u	u	u

Table 25: VSRCON Register

MODG[2:0]	PGAGS[2:0]	LN	ADCHOPEN	Gain	Differential Input Range	Common-mode Input Range	Input Impedance
000	000	0	1*	1	±VREF	-0.2V ~ADPS	10^{12} / Fadc / 增益 / 2
101	000	0	1*	2	±VREF / 2		
001	000	0	1*	4	±VREF / 4		
000	000	1	1	1	±VREF	0.4V ~ADPS-0.9V	大于 1GΩ 受 BUFCF[2:0]影响，详细见 ADCFS 寄存器说明
101	000	1	1	2	±VREF / 2		
001	000	1	1	4	±VREF / 4		
101	010	1	1	8	±VREF / 8	0.4V ~ADPS-0.9V	大于 1GΩ 受 PGACF[2:0]影响，详细见 ADCFS 寄存器说明
001	010	1	1	16	±VREF / 16		
001	011	1	1	32	±VREF / 32		
001	100	1	1	64	±VREF / 64		
001	101	1	1	128	±VREF / 128		
001	110	1	1	256	±VREF / 256		
001	111	1	1	512	±VREF / 512		

*对于前 3 种设置，可以将 ADCHOPEN 设置为 0 来提高分辨率，但此时的 OFFSET 会比较大，可以通过软件正测和反测来抵消该 OFFSET。

Table 26: ADC Gain Configuration

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1A1	ADCFS	-	ADC_RESULT_SEL	BUFCF[2:0]			PGACF[2:0]		
R/W		-	y	y	y	y	y	y	y
AsyReset		-	0	0	1	0	0	1	0
SynReset		-	u	u	u	u	u	u	u

Table 27: ADCFS Register

PGACF[2:0]----PGA Chopper Frequency Set，default 010
BUFCF[2:0]----Buffer Chopper Frequency Set，default 010
对输入阻抗要求特别高的场合，请将 PGACF[2:0]和 BUFCF[2:0]设置为 000 或 111，但噪声性能会有下降，请折中处理。
对输入阻抗要求不是特别高的场合，请将 PGACF[2:0]和 BUFCF[2:0]保持为默认值 010。

PGACF[2:0]	fPGA	BUFCF[2:0]	fBuf
000	固定高电平	000	固定高电平
001	fs/16	001	fs/16
010	fs/32（默认）	010	fs/32（默认）
011	fs/64	011	fs/64
100	fs/128	100	fs/128
101	fs/256	101	fs/256
110	fs/512	110	fs/512
111	固定低电平	111	固定低电平

4.14.3 ADC 的基准设置

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x19F	VREFSEL	-	--		MODG0	VRS[3:0]			
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	0	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 28: ADC Reference Configuration Register

Bit7~Bit5，请保持为 0。
MODG0 的说明参考**表 26 ADC Gain Configuration**。
VRS[3:0]：ADC 基准电压选择，请参考**表 29 ADC Reference Voltage**。

VRS[3:0]	LN	ADC 基准正端 VRP	ADC 基准负端 VRN	VRP-VRN
0000	X	VSR	VSS	VSR，输入无 Buffer（默认）
0001	X	ACM	VSS	ACM，输入无 Buffer
0010	0	ACM	VSS	ACM，ACM 有 Buffer
0011	X	AI2	AI3	外部决定，输入无 Buffer
0100	0	AI2	AI3	外部决定，输入有 Buffer
0101	X	AI2	VSS	外部决定，输入无 Buffer
0110	0	AI2	VSS	外部决定，AI2 有 Buffer
0111	X	AI3	VSS	外部决定，输入无 Buffer
1000	0	AI3	VSS	外部决定，AI3 有 Buffer
VRS[3:0]	LN	ADC 基准正端 VRP	ADC 基准负端 VRN	VRP-VRN
1001	X	VSR	AI2	外部决定，输入无 Buffer
1010	0	VSR	AI2	外部决定，AI2 有 Buffer
1011	X	VSR	AI3	外部决定，输入无 Buffer
1100	0	VSR	AI3	外部决定，AI3 有 Buffer
1101-1111	X	保留未用		

Table 29: ADC Reference Voltage

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1A0	HBS	VCPS[4]	--				ACMS[4:0]		
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	1	0	0	1	0
SynReset		u	u	u	u	u	u	u	u

Table 30: HBS Register

ACMS[4:0]——ACM 输出电压设置，常规应用请设置为 00000（1.20V）。

ACMS[4:0]	ACM 电压值
00000	内部 BG 电压值（1.20V）
00001~11111	VSR/32×1 ~ VSR/32×31（最大输出电压不能超过 VSR - 1.0V）

BIT6 和 BIT5 必须设置为 0。

4.14.4 ADC 的输出数据速率设置

ADC 带有 3 阶数字滤波器和高通滤波器，24 位数据输出，输出的数据带有符号：

- 正数范围为 0x000000~0x7FFFFF；
- 负数范围为 0x800000~0xFFFFFF，其中 0xFFFFFF 为-1。

在 ADC 使能或者 ADC 设置改变后，请对 FILT_RST 位先置 1 再清 0 来复位数字滤波器，数字滤波器复位后，第 3 笔数据有效。

```
bsf     ADCON3,FILT_RST,0     ;reset adc's filter bcf     ADCON3,FILT_RST,0
bcf     ADCON3,FILT_RST,0
```

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x19D	ADCON3	OSR[3:0]				ADCK_SEL[2:0]			FILT_RST
R/W		y	y	y	y	y	y	y	y
AsyReset		0	1	1	0	0	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 31: ADC Control Register 3

FILT_RST：
数字滤波器复位，对该位先置 1 再清 0 即可复位数字滤波器。
ADC 使能或者设置改变后，请对数字滤波器进行复位，复位后第 3 笔数据有效。
OSR[3:0]：ADC 的过采样率 OSR 选择

OSR[3:0]	过采样率	OSR[3:0]	过采样率	OSR[3:0]	过采样率
0000	64	0100	1024	1000	16384
0001	128	0101	2048	1001	32768
0010	256	0110	4096	1010	65536
0011	512	0111	8192	1011~1111	--

ADCK_SEL[2:0]：ADC 的工作频率 Fadc 选择

ADCK_SEL[2:0]	时钟

111	TIMER-C 设置，$F_{adc} = F_{Hrc\_clk} / (2 \times (Tmc\_data + 1))$
110	Per_clk / 2 (16kHz)
101	Hrc_clk / 78(102.5kHz)（MCU 的工作时钟 mcu_clk 需大于等于 2MHz）
100	Hrc_clk / 48(166.7kHz)（MCU 的工作时钟 mcu_clk 需大于等于 2MHz）
011	Hrc_clk / 128 (62.5kHz)
010	Hrc_clk / 64 (125kHz)
001	Hrc_clk / 32 (250kHz)
000	Hrc_clk / 16 (500kHz) （MCU 的工作时钟 mcu_clk 需大于等于 2MHz）

ADC 的数据输出速率 Fsps = Fadc / OSR。
数据输出速率 Fsps 越低，ADC 的有效位数越高，在实际的应用过程中请对 Fsps 进行合理的选择。下表就常见的一些应用推荐了数据输出速率。

应用场合	$F_{sps} = F_{adc} / OSR$	备注
高精度测量	15sps = 500kHz / 32768	
	10sps = 166.7kHz / 16384	对 50Hz 和 60Hz 干扰有抑制作用
快速测量	1.3ksps = 166.7kHz / 128	
温度传感器	122sps = 500kHz / 4096	
电池检测	122sps = 500kHz / 4096	

Table 32: 常见 ADC 数据输出速率

4.14.5 温度测量说明

温度的测量，需要按照如下步骤进行设置和测量:

- MODG[2:0]设置为 000，PGAGS[2:0]设置为 000;
- LN 设置为 1，ADCHOPEN 设置为 1;
- 基准选择 VSR 和 VSS，VSR 设置为 2.4V;
- ADC 时钟设置为 500kHz，OSR 设置为 4096;
- 设置 ADC 的通道设置为 TSP 和 TSN;
- 开启 ADC;
- 将 FILT_RST 位置 1，然后将 FILT_RST 位置 0，两条指令之内完成;
- 获取第 3 笔数据的 ADC 结果，保存;
- 设置 ADC 的通道设置为 TSN 和 TSP;
- 将 FILT_RST 位置 1，然后将 FILT_RST 位置 0，两条指令之内完成;
- 获取第 3 笔数据的 ADC 结果;
- 将之前保存的 ADC 结果减去本次 ADC 结果，得到最终的 ADC 数据。

具体的温度测量和计算方法，请参考《08XX 内部硅温度传感器应用笔记》。

4.14.6 Σ-Δ ADC 结果寄存器

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x198	ADCRTH	adc_result[23:16]							
R/W		r	r	r	r	r	r	r	r
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 33: Σ-Δ ADC 结果寄存器 24 位的最高 8 位

读 ADC 结果 adc_result[23:16]。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x199	ADCRTM	adc_result[15:8]							
R/W		r	r	r	r	r	r	r	r
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 34: Σ-Δ ADC 结果寄存器 24 位的中间 8 位

读 ADC 结果 adc_result[15:8]。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x19A	ADCRTL	adc_result [7:1]							adc_result[0] CPCKS[2]
R/W		r	r	r	r	r	r	r	y
AsyReset		x	x	x	x	x		0	0
SynReset		u	u	u	u	u	u	u	u

Table 35: Σ-Δ ADC 结果寄存器 24 位的最低 8 位

（写操作时只能用赋值语句操作）

读 ADC 结果 adc_result[7:0]，其中写 BIT0 为写 CPCKS[2]。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1A1	ADCFS	-	ADC_RESULT_SEL	BUFCF[2:0]			PGACF[2:0]		
R/W		-	y	y	y	y	y	y	y
AsyReset		-	0	0	1	0	0	1	0
SynReset		-	u	u	u	u	u	u	u

Table 36: ADCFS Register

ADC_RESULT_SEL：ADC 结果选择

“1”读 adc_result[23:0]，读到的是 Σ-Δ ADC 输出经过高通的结果；

“0”读 adc_result[23:0]，读到的是 Σ-Δ ADC 输出的直接结果，默认。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x10	ADD_RESULT0	add_result [7:0] / add_result [31:24]							
R/W		r	r	r	r	r	r	r	r
AsyReset		x	x	x	x	x	x	x	x
Address	**Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
SynReset		u	u	u	u	u	u	u	u

Table 37: 累加结果寄存器 0

读累加结果 add_result[7:0]（INTSEL 寄存器的 ADD_RESULT_SEL 为 0）或 add_result[31:24]（INTSEL 寄存器的 ADD_RESULT_SEL 为 1）。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x11	ADD_RESULT1	add_result[15:8] / add_result [39:32]							
R/W		r	r	r	r	r	r	r	r
AsyReset		x	x	x	x	x	x	x	x

SynReset	u	u	u	u	u	u	u	u

Table 38: 累加结果寄存器 1

读累加结果 add_result[15:8]（INTSEL 寄存器的 ADD_RESULT_SEL 为 0）或 add_result[39:32]（INTSEL 寄存器的 ADD_RESULT_SEL 为 1）。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x12	ADD_RESULT2	add_result [23:16] / add_result [47:40]							
R/W		r	r	r	r	r	r	r	r
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 39: 累加结果寄存器 2

读累加结果 add_result[23:16]（INTSEL 寄存器的 ADD_RESULT_SEL 为 0）或 add_result[47:40]（INTSEL 寄存器的 ADD_RESULT_SEL 为 1）。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1B	INTSEL	--		I2C_SEL	ADD_RESULT_SEL	INT3_SEL[1:0]		INT2_SEL[1:0]	
R/W		--	y	y	y	y	y	y	y
AsyReset		--	0	0	0	0	1	1	1
SynReset		--	u	u	u	u	u	u	u

ADD_RESULT_SEL：读累加器结果（ADD_RESULT[2:0]）高低 24bits 选择

“0”读累加器的低 24bits（add_result[23:0]），默认；

“1”读累加器的高 24bits（add_result[47:24]）。

4.14.7 ADC 数据平方和累加功能

数字滤波器具有高通、平方和累加三个功能，以下就这 3 个功能的组合进行描述：

1 Σ-Δ ADC 的结果（adc_result[23:0]），经过高通后再进行平方和累加，可以做交流 RMS 运算，设置如下：

1.1 将 CICCON 寄存器的 ADDSEL 位置 0，X2SEL 位置 0，HPEN 位置 1，根据需要选择高通的系数（HPCF 位）；

1.2 将 PT4SREN 寄存器的 ADD_ADC_SEL 位置 0，选择 Σ-Δ ADC；

1.3 根据实际的需求，向 ADD_COUNT 寄存器设置合适的累加次数；

1.4 将 TCON2 寄存器的 ADCIF_SEL 位置 1，将 ADCIF 中源选择为累加和中断；

1.5 将 EXTCON 寄存器的 ADDEN 位置 1，开始累加，累加的结果存放在 add_result[47:0]中。

2 Σ-Δ ADC 的结果（adc_result[23:0]），直接进行平方和累加，可以做 RMS 运算，设置如下：

2.1 将 CICCON 寄存器的 ADDSEL 位置 0，X2SEL 位置 1，HPEN 位置 0；

2.2 将 PT4SREN 寄存器的 ADD_ADC_SEL 位置 0，选择 Σ-Δ ADC；

2.3 根据实际的需求，向 ADD_COUNT 寄存器设置合适的累加次数；

2.4 将 TCON2 寄存器的 ADCIF_SEL 位置 1，将 ADCIF 中源选择为累加和中断；

2.5 将 EXTCON 寄存器的 ADDEN 位置 1，开始累加，累加的结果存放在 add_result[47:0]中。

3 Σ-Δ ADC 的结果（adc_result[23:0]），直接进行累加，可以做低通处理，设置如下：

3.1 将 CICCON 寄存器的 ADDSEL 位置 1，X2SEL 位置 1，HPEN 位置 0；
3.2 将 PT4SREN 寄存器的 ADD_ADC_SEL 位置 0，选择 Σ-Δ ADC；
3.3 根据实际的需求，向 ADD_COUNT 寄存器设置合适的累加次数；
3.4 将 TCON2 寄存器的 ADCIF_SEL 位置 1，将 ADCIF 中源选择为累加和中断；
3.5 将 EXTCON 寄存器的 ADDEN 位置 1，开始累加，累加的结果存放在 add_result[47:0]中。

4 SAR ADC 的结果（sar_result[11:0]），直接进行平方和累加，可以做 RMS 运算，设置如下：
4.1 将 CICCON 寄存器的 ADDSEL 位置 0，X2SEL 位置 1，HPEN 位置 0；
4.2 将 PT4SREN 寄存器的 ADD_ADC_SEL 位置 1，选择 SAR ADC；
4.3 根据实际的需求，向 ADD_COUNT 寄存器设置合适的累加次数；
4.4 将 TCON2 寄存器的 ADCIF_SEL 位置 1，将 ADCIF 中源选择为累加和中断；
4.5 将 EXTCON 寄存器的 ADDEN 位置 1，开始累加，累加的结果存放在 add_result[47:0]中。

5 SAR ADC 的结果（sar_result[11:0]），直接进行累加，可以做低通处理，设置如下：
5.1 将 CICCON 寄存器的 ADDSEL 位置 1，X2SEL 位置 1，HPEN 位置 0；
5.2 将 PT4SREN 寄存器的 ADD_ADC_SEL 位置 1，选择 SAR ADC；
5.3 根据实际的需求，向 ADD_COUNT 寄存器设置合适的累加次数；
5.4 将 TCON2 寄存器的 ADCIF_SEL 位置 1，将 ADCIF 中源选择为累加和中断；
5.5 将 EXTCON 寄存器的 ADDEN 位置 1，开始累加，累加的结果存放在 add_result[47:0]中。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1CC	CICCON	ADDSEL	-	ADCCNT_SEL	HPCF	SPI_SYN	X2SEL	HPEN	-
R/W		y	-	y	y	y	y	y	-
AsyReset		0	-	0	0	0	0	0	-
SynReset		u	-	u	u	u	u	u	-

ADDSEL：累加源选择。
HPCF：高通稳定速度选择
“0”稳定速度快；
“1”稳定速度慢。
X2SEL：平方选择
HPEN：高通使能
“1”高通使能
“0”高通关闭

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1CB	PT4SREN	---			SPI_SEL	PT4SREN[3:2]		-	ADD_ADC_SEL
R/W		---			y	y	y	-	y
AsyReset		---			0	0	0	-	0
SynReset		---			u	u	u	-	u

ADD_ADC_SEL：
“0”：选择 Σ-Δ ADC 的结果（adc_result[23:0]）进行累加；
“1”：选择 SAR ADC 的结果（sar_result[11:0]）进行累加，SARCON 寄存器的 SAR_PS[1:0]需设置为“01”或“10”。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

0x1D3	ADD_COUNT	add_count[7:0]							
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	0	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 40: 累加次数寄存器

add_count：滤波器的结果或者平方后的结果累加次数，累加次数 = add_count + 1，累加后的结果存放在 add_result[47:0]。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1D4	EXTCON	ADDEN	-	-	-	-	-	-	-
R/W		y	-	-	-	-	-	-	-
AsyReset		0	-	-	-	-	-	-	-
SynReset		u	-	-	-	-	-	-	-

Table 41: EXTCON Register

ADDEN：累加使能

“0”累加关闭；

“1”累加使能。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1D2	TCON2	ADCIF_SEL	-	-	-	-	-	-	-
R/W		y	-	-	-	-	-	-	-
AsyReset		0	-	-	-	-	-	-	-
SynReset		u	-	-	-	-	-	-	-

Table 42: TCON2 Register

ADCIF_SEL：ADCIF 中断源选择

“0”Σ-Δ ADC 数据更新中断；

“1”滤波器累加结束中断。

4.14.8 输入电压与 ADC 转换结果的关系式

设 Vin 为芯片模拟输入通道的单端或者差分电压，AdcResult（24bits）为 ADC 的转换数据，Gain 为设置的增益，Vref 为 ADC 的基准。

如果 AdcResult 最高位为 0，则 Vin 和 AdcResult 之间的关系如式 14-1 所示：

$$V_{in} = \frac{AdcResult}{2^{23}} \times V_{ref} \div Gain \qquad \text{（式 14-1）}$$

如果 AdcResult 最高位为 1，则 Vin 和 AdcResult 之间的关系如式 14-2 所示：

$$V_{in} = \frac{AdcResult - 2^{24}}{2^{23}} \times V_{ref} \div Gain \qquad \text{（式 14-2）}$$

4.15 LCD/LED 驱动器-LCD/LED DRIVER

4.15.1 LCD 功能说明

1/3 BIAS，支持 1/4 DUTY 和 1/3DUTY 两种方式。

最大支持 31SEG×4COM 或者 32SEG×3COM，SEG 和 COM 都和数字 IO 复用。内置升压电路，驱动电压可以选择。

支持低功耗待机显示，将寄存器 ADCRTL 的 BIT0（CPCKS[2]）设置为 1，则可以采用 LRC 作为电荷泵的时钟。

具有闪烁控制功能，通过寄存器位 LCDBL 的控制显示关闭或者打开，从而实现闪烁的效果，设置“1”使 LCD 全灭，设置“0”使 LCD 显示，显示的内容为写入寄存器 LCDDATA15-LCDDATA0 的内容。

寄存器 LCDSEL4-LCDSEL1 选择管脚作为数字 IO 使用或 SEG 管脚使用。

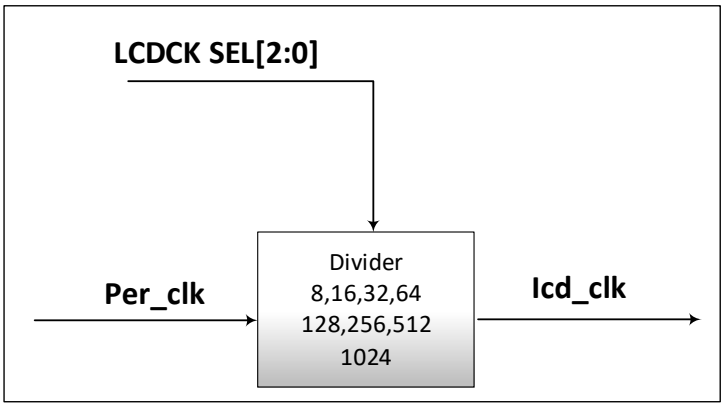

Figure 19: LCD 工作时钟

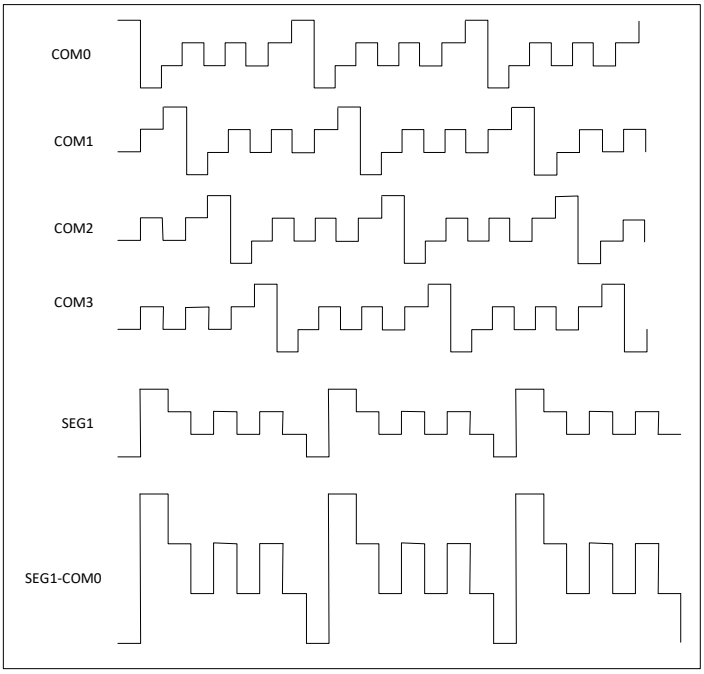

Figure 20: 1/4DUTY，1/3BIAS 时序

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDDATA0	S2C3	S2C2	S2C1	S2C0	S1C3	S1C2	S1C1	S1C0
LCDDATA1	S4C3	S4C2	S4C1	S4C0	S3C3	S3C2	S3C1	S3C0

LCDDATA2	S6C3	S6C2	S6C1	S6C0	S5C3	S5C2	S5C1	S5C0
LCDDATA3	S8C3	S8C2	S8C1	S8C0	S7C3	S7C2	S7C1	S7C0
LCDDATA4	S10C3	S10C2	S10C1	S10C0	S9C3	S9C2	S9C1	S9C0
LCDDATA5	S12C3	S12C2	S12C1	S12C0	S11C3	S11C2	S11C1	S11C0
LCDDATA6	S14C3	S14C2	S14C1	S14C0	S13C3	S13C2	S13C1	S13C0
LCDDATA7	S16C3	S16C2	S16C1	S16C0	S15C3	S15C2	S15C1	S15C0
LCDDATA8	S18C3	S18C2	S18C1	S18C0	S17C3	S17C2	S17C1	S17C0
LCDDATA9	S20C3	S20C2	S20C1	S20C0	S19C3	S19C2	S19C1	S19C0
LCDDATA10	S22C3	S22C2	S22C1	S22C0	S21C3	S21C2	S21C1	S21C0
LCDDATA11	S24C3	S24C2	S24C1	S24C0	S23C3	S23C2	S23C1	S23C0
LCDDATA12	S26C3	S26C2	S26C1	S26C0	S25C3	S25C2	S25C1	S25C0
LCDDATA13	S28C3	S28C2	S28C1	S28C0	S27C3	S27C2	S27C1	S27C0
LCDDATA14	S30C3	S30C2	S30C1	S30C0	S29C3	S29C2	S29C1	S29C0
LCDDATA15	--	--	--	--	S31C3	S31C2	S31C1	S31C0

*S1C0 表示 SEG1-COM0

Table 43: LCD 数据寄存器对应关系 - 1/4 DUTY

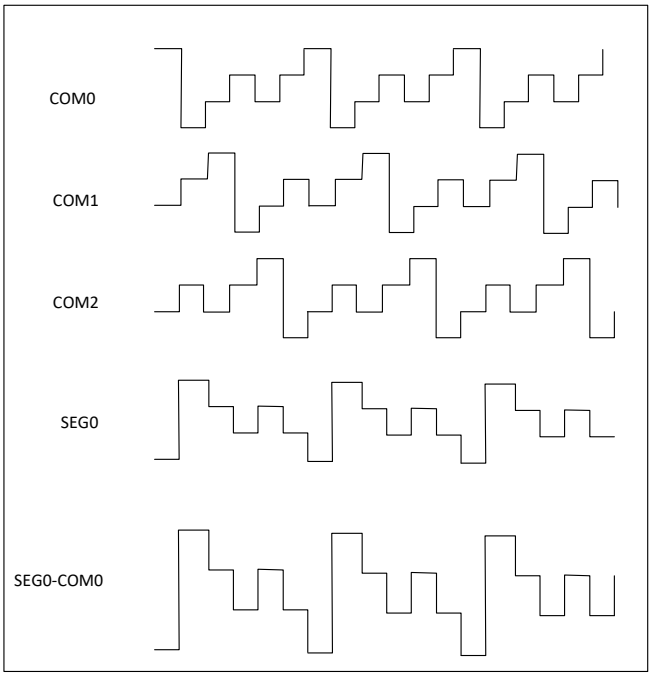

Figure 21: 1/3DUTY，1/3BIAS 时序

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDDATA0	*S0C1*	S2C2	S2C1	S2C0	*S0C0*	S1C2	S1C1	S1C0
LCDDATA1	--	S4C2	S4C1	S4C0	*S0C2*	S3C2	S3C1	S3C0
LCDDATA2	--	S6C2	S6C1	S6C0	--	S5C2	S5C1	S5C0
LCDDATA3	--	S8C2	S8C1	S8C0	--	S7C2	S7C1	S7C0
LCDDATA4	--	S10C2	S10C1	S10C0	--	S9C2	S9C1	S9C0
LCDDATA5	--	S12C2	S12C1	S12C0	--	S11C2	S11C1	S11C0
LCDDATA6	--	S14C2	S14C1	S14C0	--	S13C2	S13C1	S13C0
LCDDATA7	--	S16C2	S16C1	S16C0	--	S15C2	S15C1	S15C0
LCDDATA8		S18C2	S18C1	S18C0	--	S17C2	S17C1	S17C0
LCDDATA9	--	S20C2	S20C1	S20C0	--	S19C3	S19C2	S19C1

LCDDATA10	--	S22C2	S22C1	S22C0	--	S21C3	S21C2	S21C1
LCDDATA11	--	S24C2	S24C1	S24C0	--	S23C3	S23C2	S23C1
LCDDATA12	--	S26C2	S26C1	S26C0	--	S25C3	S25C2	S25C1
LCDDATA13	--	S28C2	S28C1	S28C0	--	S27C3	S27C2	S27C1
LCDDATA14	--	S30C2	S30C1	S30C0	--	S29C3	S29C2	S29C1
LCDDATA15	--	--	--	--	--	S31C3	S31C2	S31C1

*S0C0 表示 SEG0-COM0

Table 44: LCD 数据寄存器对应关系 - 1/3DUTY

```
1.  // 1/4 DUTY，SEG1-SEG16 使能，全显示
2.  PT3CON & = 0xF0;                    // P33~P30 intput
3.  PT3PU |= 0x0F;
4.
5.  LCDSEL1 = 0xFF;                     // SEG1~SEG8
6.  LCDSEL1 = 0xFF;                     // SEG1~SEG8
7.
8.  LCDCON = 0x00;
9.  LCDCON |= (BIT6 + BIT3);            // COM enable, 64Hz
10.
11. LCDPWR = 0x00;
12. CPBGEN = 1;
13. VCPS4 = 0;
14. LCDPWR |= (BIT7 + BIT4 + BIT3 + BIT1);  // CP = 3.02v
15.
16. LCDEN = 1;                          // LCD Driver enable
```

4.15.2 LED 功能说明

LED 驱动有两种模式：

- LED 模式 1，采用点阵驱动方式，最多使用 8 个 IO，驱动 8×7=56 个 LED。
- LED 模式 2，采用动态扫描方式，最多使用 16 个 IO，驱动 8×8=64 个 LED。

两种模式都可以通过 PWM 调节亮度，使用 PWM 调节亮度功能需将 LEDCON 寄存器的 LED_PWM 位置 1，LED_PWM1~ LED_PWM8 寄存器分别对应 1~8 段显示时的占空比，LED 模式 1 的每个寄存器只对应 7 段，所以只使用 LED_PWM1~ LED_PWM7。

具有闪烁控制功能，通过寄存器位 LCDBL 的控制显示关闭或者打开实现闪烁的效果，LCDBL 设置为“1”使 LED 全灭，LCDBL 设置为“0”使 LED 显示，显示的内容为写入寄存器 LCDDATA0-LCDDATA7 的内容。

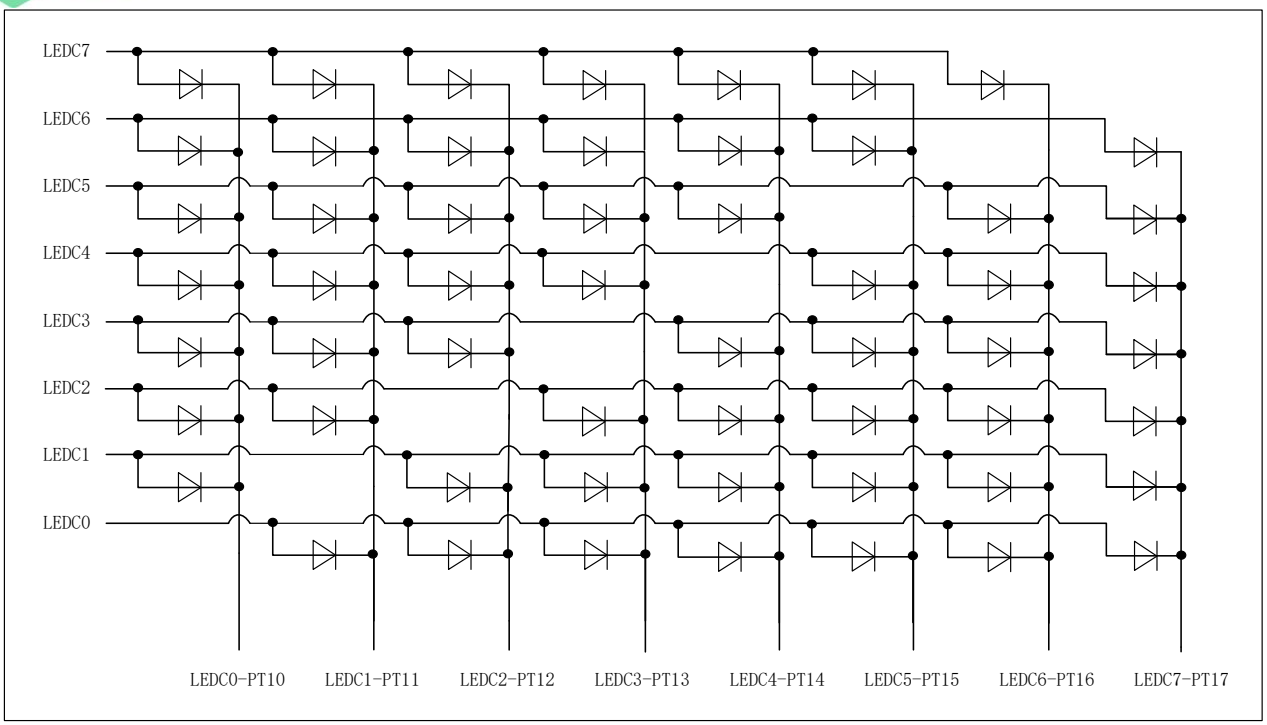

Figure 22: 扫描接线原理图（模式 1）

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDDATA0	LED70	LED60	LED50	LED40	LED30	LED20	LED10	1
LCDDATA1	LED71	LED61	LED51	LED41	LED31	LED21	1	LED01
LCDDATA2	LED72	LED62	LED52	LED42	LED32	1	LED12	LED02
	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
LCDDATA3	LED73	LED63	LED53	LED43	1	LED23	LED13	LED03
LCDDATA4	LED74	LED64	LED54	1	LED34	LED24	LED14	LED04
LCDDATA5	LED75	LED65	1	LED45	LED35	LED25	LED15	LED05
LCDDATA6	LED76	1	LED56	LED46	LED36	LED26	LED16	LED06
LCDDATA7	1	LED67	LED57	LED47	LED37	LED27	LED17	LED07

*LED 数据寄存器，LED10 表示阳极是 LEDC1，阴极是 LEDC0

Table 45: LED 数据寄存器对应关系（模式 1）

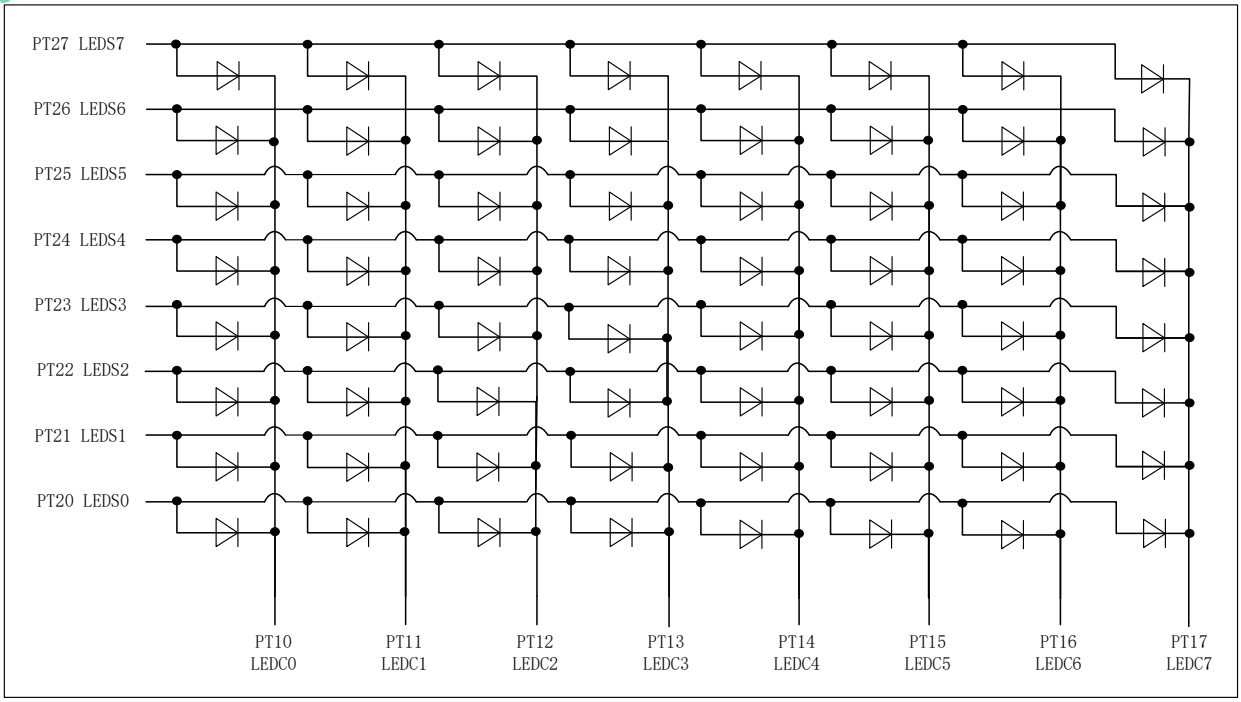

Figure 23: LED 扫描接线原理图（模式 2，共阴）

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDDATA0	S0C7	S0C6	S0C5	S0C4	S0C3	S0C2	S0C1	S0C0
LCDDATA1	S1C7	S1C6	S1C5	S1C4	S1C3	S1C2	S1C1	S1C0
LCDDATA2	S2C7	S2C6	S2C5	S2C4	S2C3	S2C2	S2C1	S2C0
LCDDATA3	S3C7	S3C6	S3C5	S3C4	S3C3	S3C2	S3C1	S3C0
LCDDATA4	S4C7	S4C6	S4C5	S4C4	S4C3	S4C2	S4C1	S4C0
LCDDATA5	S5C7	S5C6	S5C5	S5C4	S5C3	S5C2	S5C1	S5C0
LCDDATA6	S6C7	S6C6	S6C5	S6C4	S6C3	S6C2	S6C1	S6C0
LCDDATA7	S7C7	S7C6	S7C5	S7C4	S7C3	S7C2	S7C1	S7C0

*S0C0 表示 LEDS0-LEDC0

Table 46: LED 数据寄存器对应关系（模式 2）

```
1.  // 模式 2，LED 初始化和全显示
2.  PT1 = 0x00;
3.  PT2 = 0x00;
4.
5.  PT1SREN = 0xFF;
6.  PT1SREN = 0xFF;
7.
8.  PT1CON = 0xFF;                    // P17~P10 output 0
9.  PT2CON = 0xFF;                    // P27~P20 output 0
10.
11. LCDPWR = 0x00;
12. LCDCON = 0x00;
13.
14. LCDCON |= (BIT5 + BIT4);          // LEDCLK = 72Hz
15.
```

```
16. LCDDATA0 = 0xFF;
17. LCDDATA1 = 0xFF;
18. LCDDATA2 = 0xFF;
19. LCDDATA3 = 0xFF;
20. LCDDATA4 = 0xFF;
21. LCDDATA5 = 0xFF;
22. LCDDATA6 = 0xFF;
23. LCDDATA7 = 0xFF;
24.
25. LEDCON = 0xA3;                    // 模式 2, 共阴，8COM * 8SEG
```

4.15.3 寄存器说明

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1AA	LCDCON	LCDEN	LCDCK_SEL[2:0]			PCOM_NIO	IREN	DUTY	LCDBL
R/W		y	y	y	y	y	y	y	y
AsyReset		0	1	0	0	0	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 47: LCD Control Register

LCDEN：LCD 使能控制位
“1”允许工作；
“0”禁止工作。
LCDCK_SEL：LCD 的工作时钟选择
“000”Per_clk 的 8 分频；
“001”Per_clk 的 16 分频；
“010”Per_clk 的 32 分频；
“011”Per_clk 的 64 分频；
“100”Per_clk 的 128 分频；
“101”Per_clk 的 256 分频；
“110”Per_clk 的 512 分频；
“111”TIMERC 的 BUZ 驱动信号。
PCOM_NIO：COM 口使能
“1”COM 口使能（COM 使能时，请将 COM 对应的 IO 置为输入口并关闭上拉）；
“0”COM 口不使能（进入待机并关闭 COM 后，请将 COM 对应的 IO 置为输出 0）。
DUTY：DUTY 选择
“1”1/3 duty；
“0”1/4 duty。
LCDBL：显示控制
“1”不显示；
“0”显示。

LCDCK_SEL[2:0]	Frame Frequency-4COM (Hz)	Frame Frequency-3COM (Hz)	LED 扫描频率（Hz）
000	1024	1333	580
001	512	667	290
010	256	334	145
011	128	167	72

100	64	84	36
101	32	42	18
110	16	21	9
111	--	--	--

Table 48: LCD 和 LED 的工作频率

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1E7	LEDCON	LED_IO [2]	LED_MODE	LED_COMMON	LED_IO[1]	LED_IO[0]	LED_PWM	LED_EN	IO_EN
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	0	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 49: LED Control Register

LED_MODE，LED 模式选择:

“1”：LED 模式 1;

“0”：LED 模式 2。

LED_COMMON，LED 模式 2 共阴和共阳选择:

“1”：LED 模式 2 为共阴模式，需将 PT2 寄存器预设为 0xFF;

“0”：LED 模式 2 为共阳模式，需将 PT2 寄存器预设为 0x00。

LED_IO[2]	LED_IO[1]	LED_IO[0]	LED 模式 1	LED 模式 2
1	1	1	4×3 (PT10-PT13)	8SEG (PT20-PT27) × 4COM (PT10-PT13)
1	1	0	5×4 (PT10-PT14)	8SEG (PT20-PT27) × 5COM (PT10-PT14)
1	0	1	6×5 (PT10-PT15)	8SEG (PT20-PT27) × 6COM (PT10-PT15)
0	X	X	7×6 (PT10-PT16)	8SEG (PT20-PT27) × 7COM (PT10-PT16)
1	0	0	8×7 (PT10-PT17)	8SEG (PT20-PT27) × 8COM (PT10-PT17)

Table 50: LED_IO[2:0]，LED 的 IO 选择

LED_PWM，LED 驱动是否采用 PWM 调节亮度:

“1”：LED 驱动采用 PWM 调节亮度（LED 模式 1 对应的 PWM 输出脚是 P10-P17，LED 模式 2 对应的 PWM 输出脚是 P20-P27）；

“0”：LED 驱动不采用 PWM 调节亮度。

LED_EN，LED 模式使能:

“1”：LED 驱动使能;

“0”：LED 驱动关闭。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1AB	LCDPWR	VLCD_SW	CPCKS[1:0]		CPREN	VCPS[3:0]			
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	1	0	0	1
SynReset		u	u	u	u	u	u	u	u

Table 51: LCD 电源寄存器

VLCD_SW：VLCD 使用外部 VLCD 引脚的电压还是 VDD

“0”选择 VDD（LCD 应用时，进行 OTP 自烧录前，请选择此选项，避免花屏）

“1”选择 VLCD

CPREN：Charge pump 使能信号

“0”关闭模块，默认

“1”使能模块，使能之前，需将 SARCON 寄存器的 BIT0（CPBGEN）置 1。

CPCKS[2:0]：Charge pump 工作时钟选择。

其中 CPCKS[2]位于 ADCRTL 寄存器的 BIT0（只写）。

CPCKS[2:0]	工作时钟
000	Hck_clk (Default)
001	Hck_clk/2
010	Hck_clk/4
011	Hck_clk/8
1xx	Lrc_clk

VCPS[4:0]：Charge pump 电压设置寄存器控制信号。

其中 VCPS[4]为 HBS 寄存器的 BIT7。

VCPS[4:0]	VLCD 输出电压(V)	VCPS[4:0]	VLCD 输出电压(V)
00000	1.70	10000	6.03
00001	1.84	10001	6.16
00010	1.97	10010	6.29
00011	2.10	10011	6.42
00100	2.23	10100	6.56（OTP 自烧录推荐值）
00101	2.36	10101	6.69
00110	2.49	10110	6.82
00111	2.62	10111	6.95
01000	2.75	11000	7.08
01001	2.88（默认值）	11001	7.21
01010	3.02	11010	7.34
01011	3.15	11011	7.47
01100	3.28	11100	7.60
01101	3.41	11101	7.74
01110	3.54	11110	7.87
01111	3.67	11111	8.0

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1EB	SARCON	SAR_EN	SAR_SAMP	SAR_CKS[1:0]		SAR_SPT[1:0]		-	CPBGEN
R/W		y	y	y	y	y	y	-	y
AsyReset		0	0	0	0	0	0	-	0
SynReset		u	u	u	u	u	u	-	u

Table 52: SARADC 控制寄存器

CPBGEN：

“0”关闭 LCD Charge pump 基准，默认；

“1”开启 LCD Charge pump 基准，开启 Charge pump 之前需要将 CPBGEN 置 1。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1AC	LCDDATA0	详细请参考表 10.1.1、10.1.2 和 10.2.1							
R/W		y	y	y	y	y	y	y	y
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 53: LCD 数据寄存器 0 - SEG2 和 SEG1

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1AD	LCDDATA1	详细请参考表 10.1.1、10.1.2 和 10.2.1							
R/W		y	y	y	y	y	y	y	y
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 54: LCD 数据寄存器 1 - SEG4 和 SEG3

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1AE	LCDDATA2	详细请参考表 10.1.1、10.1.2 和 10.2.1							
R/W		y	y	y	y	y	y	y	y
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 55: LCD 数据寄存器 2 - SEG6 和 SEG5

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1AF	LCDDATA3	详细请参考表 10.1.1、10.1.2 和 10.2.1							
R/W		y	y	y	y	y	y	y	y
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 56: LCD 数据寄存器 3 - SEG8 和 SEG7

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1B0	LCDDATA4	详细请参考表 10.1.1、10.1.2 和 10.2.1							
R/W		y	y	y	y	y	y	y	y
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 57: LCD 数据寄存器 4 - SEG10 和 SEG9

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1B1	LCDDATA5	详细请参考表 10.1.1、10.1.2 和 10.2.1							
R/W		y	y	y	y	y	y	y	y
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 58: LCD 数据寄存器 5 - SEG12 和 SEG11

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1B2	LCDDATA6	详细请参考表 10.1.1、10.1.2 和 10.2.1							
R/W		y	y	y	y	y	y	y	y
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 59: LCD 数据寄存器 6-SEG14 和 SEG13

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1B3	LCDDATA7	详细请参考表 10.1.1 和 10.1.2							
R/W		y	y	y	y	y	y	y	y
AsyReset		x	x	x	x	x	x	x	x

SynReset	u	u	u	u	u	u	u	u

Table 60: LCD 数据寄存器 7 - SEG16 和 SEG15

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1DD	LCDDATA8	详细请参考表 10.1.1 和 10.1.2							
R/W		y	y	y	y	y	y	y	y
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 61: LCD 数据寄存器 8 – SEG18 和 SEG17

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1DE	LCDDATA9	详细请参考表 10.1.1 和 10.1.2							
R/W		y	y	y	y	y	y	y	y
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 62: LCD 数据寄存器 9 – SEG20 和 SEG19

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1DF	LCDDATA10	详细请参考表 10.1.1 和 10.1.2							
R/W		y	y	y	y	y	y	y	y
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 63: LCD 数据寄存器 10 - SEG22 和 SEG21

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1E0	LCDDATA11	详细请参考表 10.1.1 和 10.1.2							
R/W		y	y	y	y	y	y	y	y
Address	**Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 64: LCD 数据寄存器 11 – SEG24 和 SEG23

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1E1	LCDDATA12	详细请参考表 10.1.1 和 10.1.2							
R/W		y	y	y	y	y	y	y	y
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 65: LCD 数据寄存器 12 – SEG26 和 SEG25

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1E2	LCDDATA13	详细请参考表 10.1.1 和 10.1.2							
R/W		y	y	y	y	y	y	y	y
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 66: LCD 数据寄存器 13 – SEG28 和 SEG27

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

0x1E3	LCDDATA14	详细请参考表 10.1.1 和 10.1.2							
R/W		y	y	y	y	y	y	y	y
AsyReset		x	x	x	x	x	x	x	x
SynReset		u	u	u	u	u	u	u	u

Table 67: LCD 数据寄存器 14 – SEG30 和 SEG29

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1E4	LCDDATA15	--				详细请参考表 10.1.1 和 10.1.2			
R/W		--	--	--	--	y	y	y	y
AsyReset		--	--	--	--	x	x	x	x
SynReset		--	--	--	--	u	u	u	u

Table 68: LCD 数据寄存器 15 - SEG31

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1B4	LCDSEL1	Lcd_sel[8:1]							
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	0	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 69: LCD SEG/IO 选择寄存器 1

Lcd_sel[8:1]：每个位对应选择 SEG8-SEG1 为液晶 SEG 口还是数字 IO

“1”液晶 SEG 口（作为 SEG 口使用时，请将对应的 IO 置为输入口，关闭上拉）；

“0”数字 IO（LCD 驱动关闭后，请将该位设置为 0，并将对应的 IO 置为输出 0）。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1B5	LCDSEL2	Lcd_sel[16:9]							
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	0	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 70: LCD SEG/IO 选择寄存器 2

Lcd_sel[16:9]：每个位对应选择 SEG16-SEG9 为液晶 SEG 口还是数字 IO

“1”液晶 SEG 口（作为 SEG 口使用时，请将对应的 IO 置为输入口，关闭上拉）；

“0”数字 IO（LCD 驱动关闭后，请将该位设置为 0，并将对应的 IO 置为输出 0）。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1E5	LCDSEL3	Lcd_sel[24:17]							
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	0	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 71: LCD SEG/IO 选择寄存器 3

Lcd_sel[24:17]：每个位对应选择 SEG24-SEG17 为液晶 SEG 口还是数字 IO

“1”液晶 SEG 口（作为 SEG 口使用时，请将对应的 IO 置为输入口，关闭上拉）；

“0”数字 IO（LCD 驱动关闭后，请将该位设置为 0，并将对应的 IO 置为输出 0）。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1E6	LCDSEL4	--	Lcd_sel[31:25]						
R/W		--	y	y	y	y	y	y	y
AsyReset		--	0	0	0	0	0	0	0
SynReset		--	u	u	u	u	u	u	u

Table 72: LCD SEG/IO 选择寄存器 4

Lcd_sel[31:25]：每个位对应选择 SEG31-SEG25 为液晶 SEG 口还是数字 IO

“1”液晶 SEG 口（作为 SEG 口使用时，请将对应的 IO 置为输入口，关闭上拉）；

“0”数字 IO（LCD 驱动关闭后，请将该位设置为 0，并将对应的 IO 置为输出 0）。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1D5	LEDPWM1	LED_PWM1_DATA[7:0]							
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	0	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 73: LED PWM1 DATA

LED 驱动时，LCDDATAx 寄存器对应输出 1 段时的占空比，周期固定为 T_{hck_clk}×4×256。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1D6	LEDPWM2	LED_PWM2_DATA[7:0]							
R/W		y	y	y	y	y	y	y	y
Address	**Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
AsyReset		0	0	0	0	0	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 74: LED PWM2 DATA

LED 驱动时，LCDDATAx 寄存器对应输出 2 段时的占空比，周期固定为 T_{hck_clk}×4×256。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1D7	LEDPWM3	LED_PWM3_DATA[7:0]							
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	0	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 75: LED PWM3 DATA

LED 驱动时，LCDDATAx 寄存器对应输出 3 段时的占空比，周期固定为 T_{hck_clk}×4×256。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1D8	LEDPWM4	LED_PWM4_DATA[7:0]							
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	0	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 76: LED PWM4 DATA

LED 驱动时，LCDDATAx 寄存器对应输出 4 段时的占空比，周期固定为 T_{hck_clk}×4×256。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1D9	LEDPWM5	LED_PWM5_DATA[7:0]							
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	0	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 77: LED PWM4 DATA

LED 驱动时，LCDDATAx 寄存器对应输出 5 段时的占空比，周期固定为 T_{hck_clk}×4×256。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1DA	LEDPWM6	LED_PWM6_DATA[7:0]							
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	0	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 78: LED PWM6 DATA

LED 驱动时，LCDDATAx 寄存器对应输出 6 段时的占空比，周期固定为 T_{hck_clk}×4×256。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1DB	LEDPWM7	LED_PWM7_DATA[7:0]							
Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	0	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 79: LED PWM7 DATA

LED 驱动时，LCDDATAx 寄存器对应输出 7 段时的占空比，周期固定为 T_{hck_clk}×4×256。

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1DC	LEDPWM8	LED_PWM8_DATA[7:0]							
R/W		y	y	y	y	y	y	y	y
AsyReset		0	0	0	0	0	0	0	0
SynReset		u	u	u	u	u	u	u	u

Table 80: LED PWM8 DATA

LED 驱动时，LCDDATAx 寄存器对应输出 8 段时的占空比，周期固定为 T_{hck_clk}×4×256。

5 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which ST17H69 can be exposed without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the ST17H69. **Table 81** specifies the absolute maximum ratings for ST17H69.

Symbol	Parameter	Min.	Max.	Unit
Supply voltages				
VDD3		-0.3	+3.6	V
DEC			1.32	V
VSS			0	V
I/O pin voltage				
VIO		-0.3	VDD + 0.3	V
Environmental				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		3	
ESD HBM	Human Body Model Class 2		2	kV
ESD CDMQF	Charged Device Model (QFN64, 4x4 mm package)		500	V
Flash memory				
Endurance			100 000	write/erase cycles
Retention			10 years at 40 °C	
Number of times an address can be written between erase cycles			2	times

Table 81: Absolute maximum ratings

6 Operating Conditions

The operating conditions are the physical Parameters that ST17H69 can operate within as defined in **Table 82**.

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD3	Supply voltage, normal mode	1.8	3	3.6	V
tr_VDD	Supply rise time (0 V to 2.4 V)			100	ms
TA	Operating temperature (consumer)	-40	27	85	°C

Table 82: Operating conditions

7 Radio Transceiver

7.1 Radio Current Consumption

Parameter	Description	MIN	TYP	MAX	UNIT
Tx only at 0dBm	with internal DC-DC @3V		4.6		mA
Rx Only	with internal DC-DC @3V		4		mA

Table 83: Radio current consumption

7.2 Transmitter Specification

7.2.1 BLE TX

Parameter	Description	MIN	TYP	MAX	UNIT
RF Max Output Power			10		dBm
RF Min Output Power			-20		dBm
OBW for BLE 1Mbps	20dB occupy-bandwidth for BLE modulation 1Mbps		1100		KHz
OBW for BLE 2Mbps	20dB occupy-bandwidth for BLE modulation 2Mbps		2300		KHz
OBW for GFSK 500Kbps	20dB occupy-bandwidth for GFSK modulation 2Mbps		1100		KHz
OBW for GFSK 125bps	20dB occupy-bandwidth for GFSK modulation 2Mbps		1100		KHz
Error Vector Measure	Offset EVM for OQPSK modulation		0.02		
FDEV for BLE 1Mbps	Frequency deviation for GFSK modulation 1Mbps	160		250	KHz
FDEV for BLE 2Mbps	Frequency deviation for GFSK modulation 2Mbps	320		500	KHz

Table 84: BLE Transmitter Specification

7.2.2 Zigbee (IEEE 802.15.4) TX

Parameter	Description	MIN	TYP	MAX	UNIT
Output power, highest setting	Delivered to a single-ended 50 Ω load through a balun		9		dBm
Error vector magnitude	At maximum output power		2%		
Spurious emission conducted measurement	f < 1 GHz, outside restricted bands		-43		dBm
	f < 1 GHz, restricted bands ETSI		-65		dBm
	f < 1 GHz, restricted bands FCC		-76		dBm
	f > 1 GHz, including harmonics		-46		dBm
	Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)				

Table 85: Zigbee (IEEE 802.15.4) Transmitter Specification

7.3 Receiver Specification

7.3.1 BLE RX

7.3.1.1 BLE 1Mbps GFSK RX

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 1Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-99		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-6		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		7		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		45		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		22		I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3		-20		dBm
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

Table 86: BLE 1Mbps GFSK RX

7.3.1.2 BLE 2Mbps GFSK RX

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 2Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-96		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-6		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		-5		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		9		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		30		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		40		I/C dB
Parameter	**Description**	**MIN**	**TYP**	**MAX**	**UNIT**
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB

Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3	22	I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3	-20	dBm
Carrier Frequency Offset Tolerance		+-350	KHz
Sample Clock Offset Tolerance		+-120	ppm

Table 87: BLE 2Mbps GFSK RX

7.3.1.3 BLE 500Kbps GFSK RX

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 500Kbps BLE ideal transmitter, 37 Byte BER=1E-3		-100		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-4		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/-1MHz, 37 Byte BER=1E-3		10		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/-2MHz, 37 Byte BER=1E-3		45		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/-3MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/-4MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		24		I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte Ber=1E-3		-19		dBm
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

Table 88: BLE 500Kbps GFSK RX

7.3.1.4 BLE 125Kbps GFSK RX

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 125Kbps BLE ideal transmitter, 37 Byte BER=1E-3		-105		dBm

co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3	-1	I/C dB
Selectivity +- 1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3	-11	I/C dB
Selectivity +- 2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3	45	I/C dB
Selectivity +- 3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3	50	I/C dB
Selectivity +- 4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3	50	I/C dB
Selectivity +- 5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3	55	I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3	28	I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3	-18	dBm
Carrier Frequency Offset Tolerance		+- 350	KHz
Sample Clock Offset Tolerance		+- 120	ppm

Table 89: BLE 125Kbps GFSK RX

7.3.2 Zigbee (IEEE 802.15.4) RX

7.3.2.1 Zigbee 250Kbps

Parameter	Description	MIN	TYP	MAX	UNIT
Receiver sensitivity	PER = 1%		-103		dBm
Adjacent channel rejection	Wanted signal at -82dBm, modulated interferer at±5 MHz, PER = 1%		40		dB
Alternate channel rejection	Wanted signal at -82dBm, modulated interferer at±10 MHz, PER = 1%		53		dB
Channel rejection, ±15 MHz or more	Wanted signal at -82dBm, undesired signal is IEEE802.15.4 modulated channel, stepped through all channels 2405 to 2480 MHz, PER = 1%		59		dB
Blocking/desensitization,5 MHz from upper band edge	Wanted signal at -97dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		66		dB
Parameter	**Description**	**MIN**	**TYP**	**MAX**	**UNIT**
Blocking/desensitization,10 MHz from upper band edge	Wanted signal at -97dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB

Blocking/desensitization,20 MHz from upper band edge	Wanted signal at -97dBm (3 dB above the sensitivity level), CW jammer, PER = 1%	66	dB
Blocking/desensitization,50 MHz from upper band edge	Wanted signal at -97dBm (3 dB above the sensitivity level), CW jammer, PER = 1%	70	dB
Blocking/desensitization,-5 MHz from lower band edge	Wanted signal at -97dBm (3 dB above the sensitivity level), CW jammer, PER = 1%	64	dB
Blocking/desensitization,-10 MHz from lower band edge	Wanted signal at -97dBm (3 dB above the sensitivity level), CW jammer, PER = 1%	65	dB
Blocking/desensitization,-20 MHz from lower band edge	Wanted signal at -97dBm (3 dB above the sensitivity level), CW jammer, PER = 1%	67	dB
Blocking/desensitization,-50 MHz from lower band edge	Wanted signalat -97dBm (3 dB above the sensitivity level), CW jammer, PER = 1%	68	dB
Spurious emissions, 30 to 1000 MHz	Conducted measurement in a 50 Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66	>200	dBm
Spurious emissions, 1 to 12.75 GHz	Conducted measurement in a 50 Ω single-ended load. Suitable for systems targeting compliance with –62 dBm GHz EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66	100	dBm
Frequency error tolerance	Difference between center frequency of the received RF signal and local oscillator frequency	+-1	ppm
RSSI dynamic range		40	dB
RSSI accuracy		53	dB

Table 90: Zigbee (IEEE802.15.4) 250Kbps RX

7.4 RSSI Specifications

Parameter	Description	MIN	TYP	MAX	UNIT
RSSI Dynamic Range			70		dB
RSSI Accuracy	RSSI Accuracy Valid in range -100 to -30dBm		+/-2		dB
RSSI Resolution	Totally 7bit, from 0 to 127		1		dB
RSSI Period			8		us

Table 91: RSSI specifications

8 Glossary

Term	Description
AHB	Advanced High-performance Bus
AHB-AP	DAP AHB Port for debug component access thru AHB bus
AMBA	Advanced Microcontroller Bus Architecture
AON	Always-on power domain
APB	Advanced Peripheral Bus
APB-AP	DAP APB Port for debug component access thru APB bus
BROM	Boot ROM
DAP	Debug Access Port
ETM	Embedded trace module
FPU	Floating Point Unit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound, Integrated Interchip Sound
ITM	Instrumentation Trace Macrocell Unit
JTAG	Joint Test Access Group (IEEE standard)
JTAG-AP	DAP's JTAG Access Port to access debug components
JTAG-DP	DAP's JTAG Debug Port used by external debugger
J&M	Jun and Marty LLC
MPU	Memory Protection Unit
NVIC	Nested vector Interrupt Controller
PCR	Power Clock Reset controller
POR	Power on reset, it is active low in this document
RFIF	APB peripheral to interface RF block
SWD	Serial Wire DAP
SoC	System on chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access memory
TWI	Two-Wire Interface
UART	Universal Asynchronous Receiver and Transmitter
WDT	Watchdog Timer

Table 92: Glossary

9 Sample Application and Layout Guide

9.1 Sample Application (QFN64)

9.1.1 With DCDC

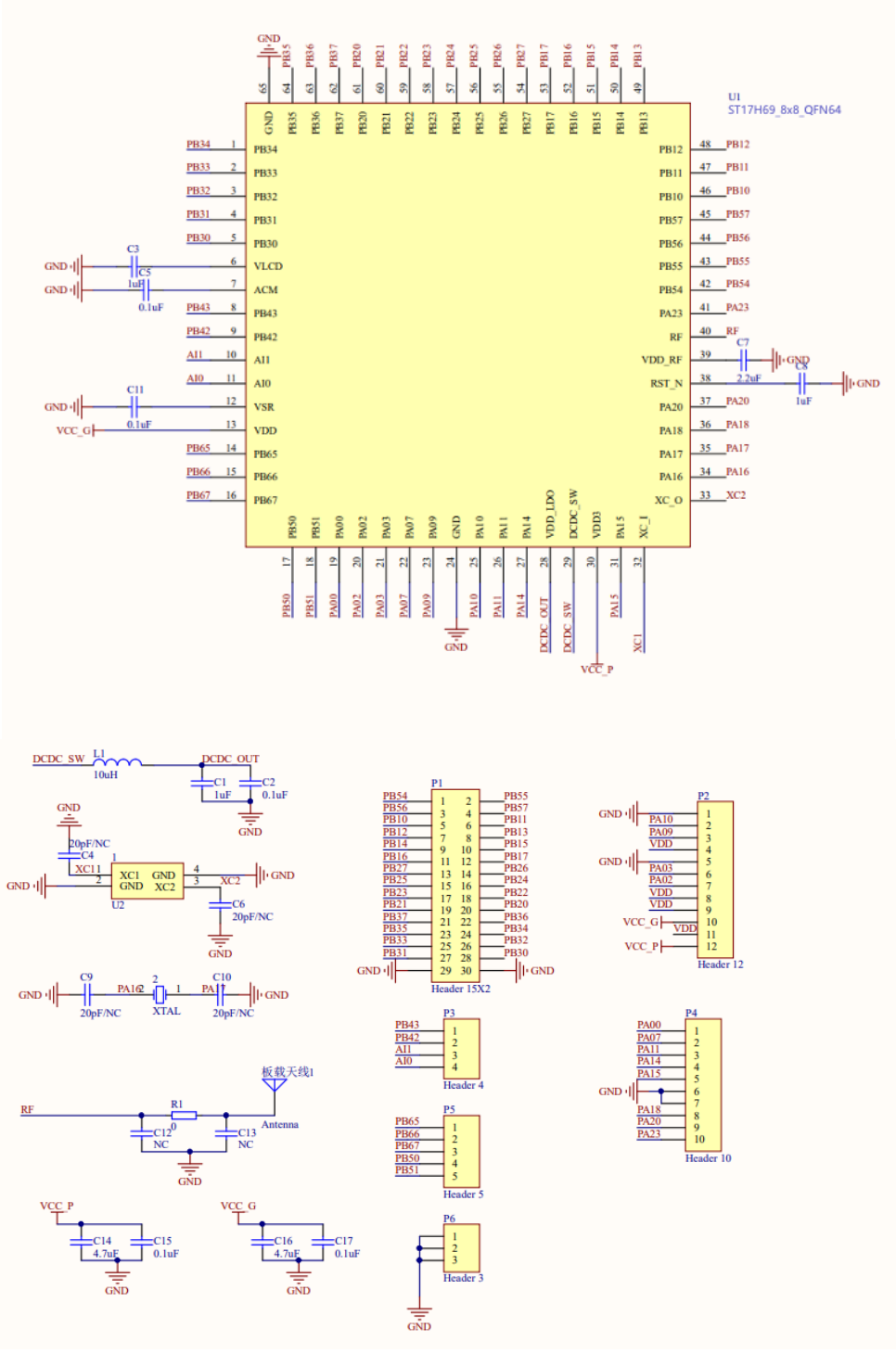

Figure 24: Sample application of QFN64 with DCDC

* If RF TX output power > 5dBm, C2=4.7uF

9.1.2 Without DCDC

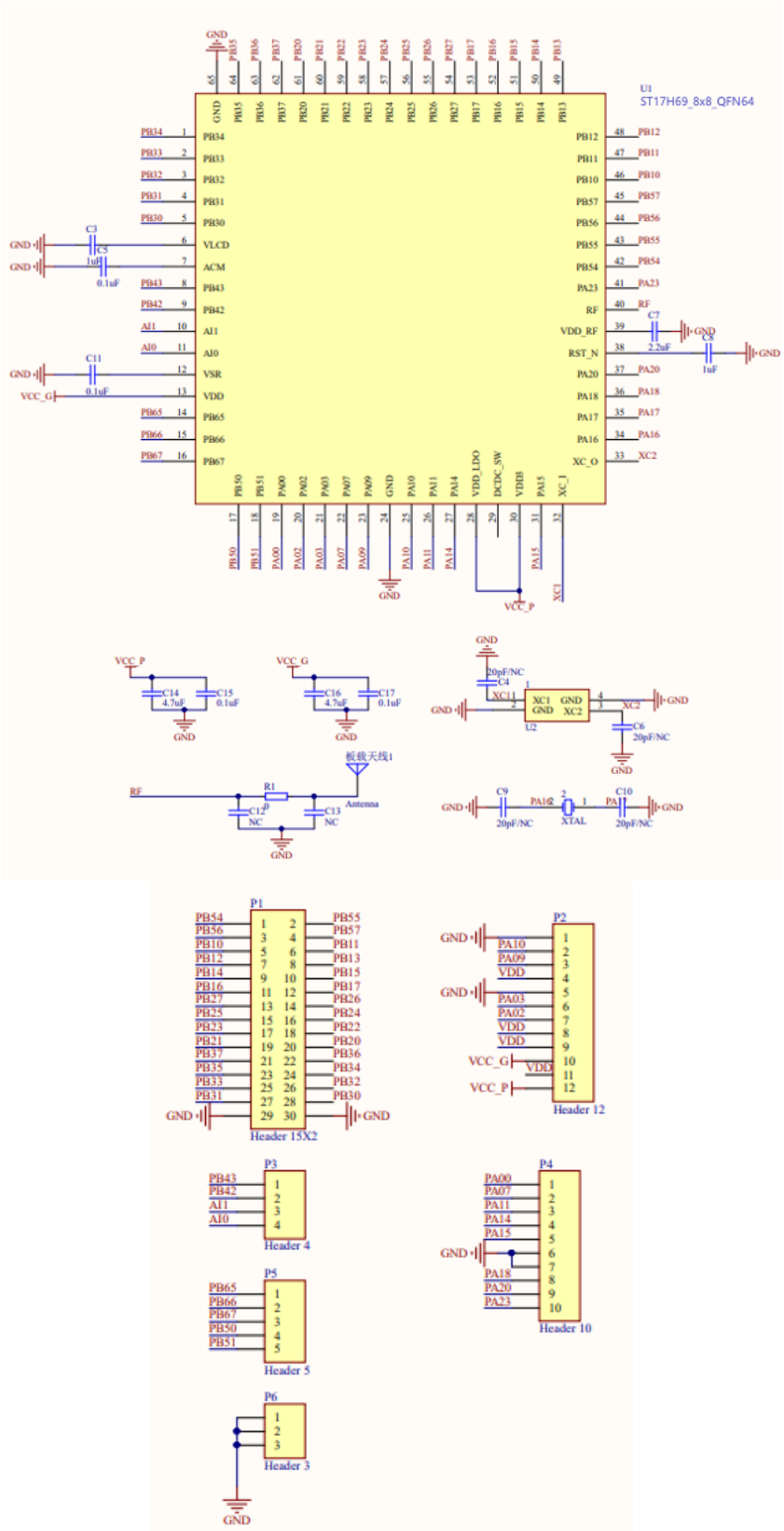

Figure 25: Sample application of QFN64 without DCDC

9.2 Layout Guide

9.2.1 Placement

1. RF matching/Loop filter leading to antenna should be isolated from any other AC/DC signal as much as possible;
2. Xtal/OSC clock is a noise source to other circuits, keep clock trace as short as possible and away from any important area;
3. LDO's are sensitive and could be easily contaminated, care should be taken for the environment;
4. Antenna is the main RF radiation point, other important blocks should be shielded or away from this area.

RF traces

1. Define RF line width with given dielectric thickness (thickness of PCB dielectric layer to ground plain) to achieve 50ohm impedance; this is mainly for the RF line connecting to matching/loop filter and antenna.
2. Differential traces should be kept in the same length and component should be placed symmetrically;
3. Certain length of RF trace should be treated as part of RF matching.

9.2.2 Bypass Capacitor

1. Each VDD pin needs a bypass capacitor to release chip internal noise and block noise from power supply.
2. For power traces, bypass capacitors should be placed as close as possible to VDD pins.
3. Use one large and one small capacitor when the pin needs two capacitors. Typically the capacitance of the larger capacitor is about 100 times of that of the smaller one. The smaller capacitor usually has better quality factor than the larger one. Place the larger capacitor closer to the pin.
4. The capacitors of Loop filter need to have larger clearance to prevent EMC/EMI issue.
5. Ground via should be close to the Capacitor GND side, and away from strong signals.

9.2.3 Layer Definition

1. Normally 4 layer PCB is recommended.
2. RF trace must be on the surface layer, i.e. top layer or bottom.
3. The second layer of RF PCB must be "Ground " layer , for both signal ground and RF reference ground , DO NOT put any other trace or plane on second layer, otherwise "antenna effect" will complicate debug process.
4. Power plane generally is on the 3rd layer.
5. Bottom layer is for "signal " layer.
6. If two layer PCB is used, quality will degrade in general. More care needs to be taken. Try to maximize ground plane, avoid crossing of signal trace with other noise lines or VDD, shield critical signal line with ground plane, maximize bypass capacitor and number of ground vias.

9.2.4 Reference clock and trace

1. Oscillator signal trace is recommended to be on the 1st layer;
2. DO NOT have any trace around or across the reference clock (oscillator) trace.
3. Isolate the reference clock trace and oscillator by having more GND via around.
4. DO NOT have any other traces under the Oscillator.

9.2.5 Power line or plane

1. Whether to use power plain or power line depend on the required current, noise and layout

condition. For RF chip, we generally suggest to use power line to bring power into IC pin. Line has parasitic inductance, which forms a low pass filter to reduce the noise traveling around PCB.

2. Add more conductive via on the current source, it will increase max current limit and reduce inductance of via.
3. Add some capacitor alone the power trace when power line travels a long distance.
4. DO NOT place power line or any plane under RF trace or oscillator and its clock trace , the strong clock or RF signal would travel with power line.

9.2.6 Ground Via

1. Ground Via must be as close to the ground pad of bypass capacitor as possible , too much distance between via and ground pad will reduce the effect of bypass capacitor.
2. Having as many ground via as possible.
3. Place ground via around RF trace, the RF trace should be shielded with via trail.